

Leakage current testing system applied to photovoltaic inverters – design and simulation

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Abstract — Grid-tied photovoltaic inverters have several challenges concerning user safety. For instance, transformerless inverters may have high common-mode leakage current due to parasitic capacitance between photovoltaic modules and ground, making electric shocks detection difficult. Inverters must be submitted to several tests to certify its compliance with safety standards. This manuscript addresses the insulation resistance test and residual current tests described in safety standard IEC 62109-2. A variable RC load that can be used for both tests is designed and its functionality is demonstrated by simulation results.

Keywords— Leakage current, Photovoltaic Inverter, Residual current, Standard Compliance, Variable load.

I. INTRODUCTION

Transformerless Photovoltaic (PV) Inverters have been widely adopted in order to increase efficiency and reduce PV system costs. This brings up an issue related to user safety for some transformerless inverter topologies: high levels of common-mode leakage current [1]. This leakage current flows through the PV parasitic capacitance between dc terminals and grounded module aluminum frame, and closes its path through inverter ac output and grid neutral. It increases safety risks because interferes with the detection of electric shock and can cause fire hazard.

This leakage current is composed of low frequency and high frequency components. The low frequency components are not filtered because they require the use of impractical large filters [2], while the high frequency components can be filtered through common-mode filters. To minimize safety issues, standard IEC 62109-2 [3] defines requirements and testing procedures for grid-tied PV inverters.

Inverter leakage current test systems are not largely addressed in literature. The leakage current test procedures indicated by IEC 62109-2 require a variable RC load. Patents [4-8] employ different load variation methods to perform this test, such as electromechanical rheostats, semiconductors operating in the linear region and mechanical switching between fixed loads. In [9], the author proposes a variable resistive load using binary weighed resistances to perform dynamic tests of power sources. In [10], a resistive load with binary weighed resistances was used to control the frequency of a Micro-hydro generator.

The objective of this manuscript is to propose a PV inverter test system different from patents [4-8], addressing two groups of tests required by IEC 62109-2: insulation resistance test and leakage current tests. The proposed solution is comprised of an electronically controlled variable RC load, with binary weighed resistances and capacitances, similar to the loads of [9] and [10], using semiconductor switching devices. This load control method is different from those claimed in the registered patents [4-8], and has the advantage of digitally control both resistance and capacitance. Simulation results demonstrate the efficacy of the solution. Some problems are discussed for the final assembly of the proposed RC load.

II. LEAKAGE CURRENT IN TRANSFORMERLESS PV INVERTERS

In the transformerless inverter topology of Fig. 1, the average dc side common-mode voltage is equal to the ac side common-mode voltage, which is half of the sinusoidal grid voltage. Therefore, this common-mode voltage together with parasitic capacitances between the photovoltaic modules and ground causes leakage currents during inverter operation. The value of the parasitic capacitances depend on factors such as the structure of the photovoltaic panels, surface of the cells, distance between the cells, weather conditions, dirt and EMI filter topology [11]. Excessive leakage current causes electric shock and fire hazards, and interferes with the quality of energy generated by the photovoltaic system. Fig. 1 shows the schematic of a full-bridge inverter including the parasitic capacitances. The variables shown in Fig. 1 are: v_{S3} and v_{S4} are the voltages on switches S_3 and S_4 , respectively; v_{PV} is the voltage on the DC bus of the PV system; v_{PV+} and v_{PV-} are the common-mode voltages between each of the photovoltaic module's poles and ground; v_{ge} is the grid voltage; and i_{cm} is the leakage current.

Considering the leakage current high frequency components are properly filtered, v_{S3} and v_{S4} average voltages are composed of a dc added to an ac component [2], and are given by:

$$v_{S3} = \frac{1}{2}(v_{PV} + v_{ge}) \quad (1)$$

$$v_{S4} = \frac{1}{2}(v_{PV} - v_{ge}) \quad (2)$$

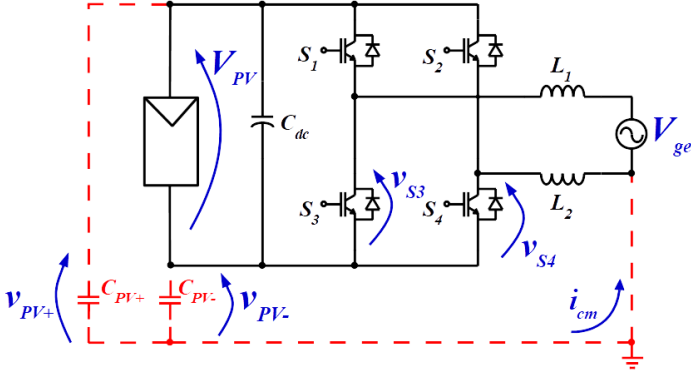


Fig. 1. Full-bridge inverter with split output inductor. The parasitic capacitances are included.

Fig. 2 shows the simplified model of PV system disregarding high-frequency components. From this circuit, v_{PV+} and v_{PV-} are calculated by (3) and (4). These voltages present a dc component equals to half of input voltage v_{pv} , and an ac component equals to half of the mains voltage v_{ge} .

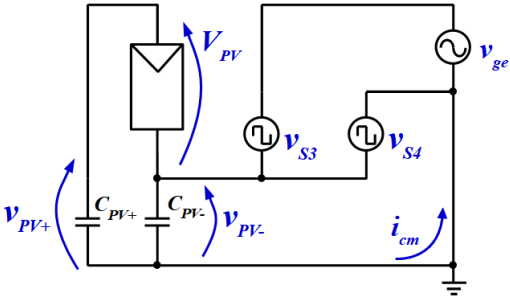


Fig. 2. Simplified model of transformerless PV inverter disregarding high-frequency components.

$$v_{PV+} = \frac{1}{2}v_{ge} + \frac{1}{2}v_{PV} \quad (3)$$

$$v_{PV-} = \frac{1}{2}v_{ge} - \frac{1}{2}v_{PV} \quad (4)$$

The leakage current flows through the parasitic capacitance of the PV panels due to the ac components on inverter input. Thus, the leakage current is calculated by (5), where f is the grid frequency and C_{PV} is the total parasitic capacitance of the PV array.

$$i_{cm} = \pi \cdot f \cdot C_{PV} \cdot v_{ge} \quad (5)$$

III. STANDARD IEC 62109-2

Standard IEC 62109 presents security requirements and testing procedures for off-grid and grid-tie PV inverters. Two important requirements of this standard are explained in the following.

A. Array insulation resistance

For transformerless inverters, the standard requires that the dc side is not directly grounded, and before connecting to the grid, the inverter must measure the resistance between the input of the PV array and ground. If the value of the measured insulation resistance is less than $(V_{PV,max} / 30 \text{ mA}) \Omega$, where $V_{PV,max}$ is the inverter's maximum input voltage, it shall indicate the occurrence of a fault and not connect to the grid. Thus, some problems can be avoided, such as improper grounding of dc side, insulation failure, electric shock caused by human contact, among others. The inverter can connect to the grid if the resistance recovers to a value higher than the limit.

The test to verify the compliance of the inverter with this requirement consists of connecting a resistance between the terminals of the PV array and ground. The inverter complies with the standard if it indicates the insulation fault and does not connect when the inserted resistance is lower than the limit. The test system shown in Section IV can be used to perform this test.

B. Leakage current

Transformerless inverters must provide continuous monitoring of the rms value of leakage current while connected to the grid. The inverter must disconnect in the occurrence of two types of faults: i) continuous rms leakage current exceeding the limit; ii) leakage current sudden change above limits.

i) Continuous leakage current: excessive continuous leakage current can create fire hazard. Inverters with power rating up to 30 kVA must disconnect when the measured rms leakage current is greater than 300 mA. Inverters with power rating greater than 30 kVA must disconnect when a continuous leakage current greater than 10 mA per kVA of rated power is measured. Disconnection shall occur within 0.3 s and the inverter must indicate the fault. It can reconnect to the grid if an insulation resistance greater than the limit is measured.

ii) Sudden leakage current change: ungrounded PV arrays can create a shock hazard if there is human contact with live parts. The shock causes a sudden increase in the leakage current, named touch current. The inverter shall disconnect from the grid if it detects a sudden increase in the rms leakage current. The maximum response times defined by the standard are presented in Table 1. These time limits depend on the amplitude of the sudden change in the current. The inverter may reconnect to the grid if the measured insulation resistance is above the limit.

TABLE I. RESPONSE TIME LIMITS, DEFINED BY THE STANDARD, DUE TO SUDDEN CHANGES ON THE LEAKAGE CURRENT

| Amplitude of the change | Maximum time for disconnection |
|-------------------------|--------------------------------|
| 30 mA | 0.3 s |
| 60 mA | 0.15 s |
| 150 mA | 0.04 s |

The test setup to verify the compliance with these requirements is shown in Fig. 3. The procedure for testing transformerless PV inverters protection against excessive continuous leakage current is:

- a) An adjustable resistance is connected between ground/neutral and one of the inverter input terminals;
- b) The resistance is slowly reduced until the inverter leakage current exceeds the maximum limit and the inverter disconnects from the grid. The rms current value which the inverter disconnected (trip level) must be registered;
- c) The resistance is adjusted to conduct a leakage current of approximately 10 mA lower than the trip level;
- d) After the inverter restarts operation, another resistance is connected in parallel, adjusted to conduct a leakage current of approximately 20 mA.

The trip level of the inverter under test is determined in step "b", which must be lower than the level defined in the standard. The response time of the inverter is obtained in step "c". This time must be measured from the moment the second resistance is inserted until the moment the inverter disconnects.

To test the protection against sudden changes of leakage current, the procedure is as follows:

- a) A variable capacitor is connected between one of the input terminals of the inverter and ground;
- b) The capacitance value is increased until the inverter disconnects from the grid due to excessive continuous leakage current. This current trip level shall be registered;
- c) The capacitance is then reduced such that the continuous leakage current equals the trip level minus 150% of the current sudden change being tested. For testing the 30 mA sudden change, the initial continuous current shall be 45 mA below the trip level. If the obtained trip level is 300 mA, the capacitance shall be adjusted to conduct 255 mA;
- d) After the inverter restarts operation, a variable resistance, adjusted to conduct 30 mA (60 mA or 150 mA) is connected in parallel with the capacitor.

The response time of the inverter protection must be measured from the moment the resistance is connected until the moment the inverter disconnects. The test shall be repeated for the three current sudden change values defined in Table I (30 mA, 60 mA and 150 mA).

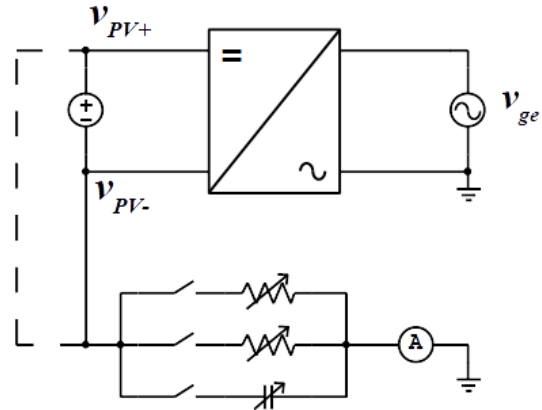


Fig. 3. Setup for leakage current testing according to IEC 62109-2.

IV. PROPOSED TEST SETUP

The proposed solution is comprised of an electronically controlled variable RC load, a calibrated equipment for current measurement and a supervisory system for interconnecting the components, offering a human-machine interface. The developed hardware is able to test the requirements presented in Sections III-A and III-B.

A. Variable RC load

In [8], an electronically controlled variable resistance, using 8 binary weighed resistors connected in series. If the first resistor has R ohms, the subsequent resistors have $2 \cdot R$, $4 \cdot R$, $8 \cdot R$, and so on. With 8 resistors it is possible to have $2^8 = 256$ different combinations of resistances. Here, the same binary logic is applied to implement a resistive and a capacitive load, but using parallel connection.

Fig. 4 shows the proposed variable RC load scheme. The resistive part of the load is composed of 8 resistors connected in parallel, with semiconductor switches to control the conduction of each resistor. The capacitive part of the load is similar to the resistive, with 8 capacitors placed in parallel, and semiconductor switches to control the conduction of each capacitor. v_{cm} is the voltage between one of the inverter input terminals and ground.

The values of the R_n resistances in the circuit of Fig. 4(a) are calculated by (6), and the C_n capacitances in Fig. 4(b) by (7). R and C are the base resistance and capacitance for the calculation of the resistors and capacitors used in the circuit. $d_{R,n}$ and $d_{C,n}$, represent the state of each switch on the circuit, they may assume the values 0 (open switch) and 1 (closed switch). The leakage current flowing through the resistive and capacitive loads are calculated by (8) and (9), respectively. The total leakage current through the RC load is the sum of the currents in each load, as in (10).

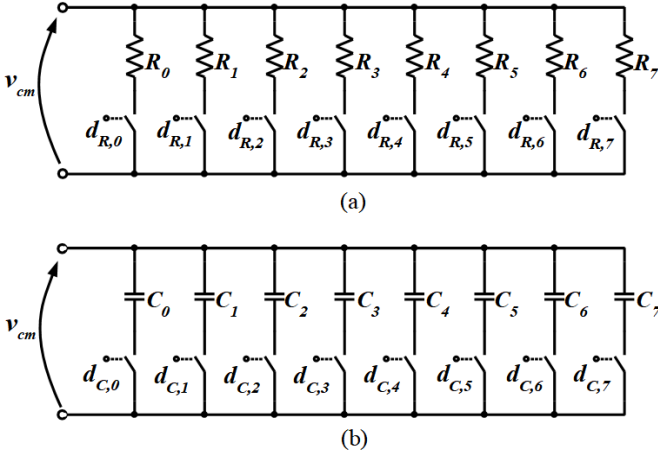


Fig. 4. Proposed RC load circuit: (a) Resistive load, (b) Capacitive load.

$$R_n = R / 2^n \quad (6)$$

$$C_n = C \cdot 2^n \quad (7)$$

$$i_{cm,rms,R} = \sum_{n=0}^7 \left[v_{cm,rms} \cdot d_{R,n} \cdot \frac{2^n}{R} \right] \quad (8)$$

$$i_{cm,rms,C} = \sum_{n=0}^7 \left[v_{ge,rms} \cdot \pi \cdot f \cdot d_{C,n} \cdot C \cdot 2^n \right] \quad (9)$$

$$i_{cm,rms,C} = i_{cm,rms,C} + i_{cm,rms,C} \quad (10)$$

Thus, the resistive and capacitive loads may have 256 different equivalent resistances and capacitances, which can continuously change depending on the state of the semiconductor switches.

B. RC load control

Semiconductor devices are used to switch the resistances and capacitances. The leakage current through the resistive load can be either unidirectional or bidirectional, depending on the dc amplitude of the common mode voltage. Therefore, a bidirectional switch must be used. The suitable switch to control the resistive load is composed of two MOSFETs, arranged in such a way that bidirectional current is allowed to flow and a full turn-off control is obtained. Fig. 5 shows the used bidirectional switch, and Fig. 6(a) shows the variable R load with the adopted switches.

On the other hand, triacs have been adopted as switch for the capacitive load, as shown in variable C load shown in Fig. 6(b). The circuit could be simplified because a common reference could be used, and the triacs can be turned off because the current crosses zero 120 times per second.

The topology of the proposed RC load presents some issues related to the moment in which its resistive and capacitive

elements are switched. In the resistive load, an important challenge is to adjust the MOSFET turn-on and turn-off times to be equal, in order to avoid current spikes when switching resistances. To solve this problem, the gate driver circuit of the MOSFETs must allow the adjustment of their turn-on and turn-off times. These times depend on the characteristics of the MOSFET being used and on the resistance of the resistor in series with it. The designed gate driver circuit, that allows the adjustment of these times, is shown in Fig. 5. The values of the resistances in the circuit must be defined experimentally. R_{on} resistors determine the turn-on time, and R_{off} the turn-off time of the MOSFETs. v_g is the gate switching signal for the MOSFETs.

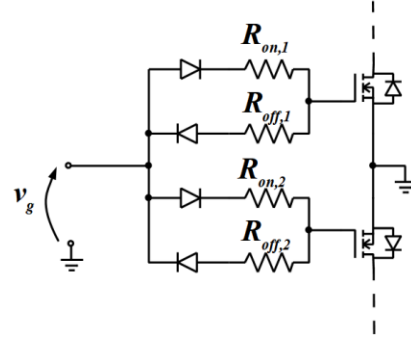


Fig. 5. Gate driver circuit for the MOSFETs: a bidirectional switch to control the resistive load.

Similarly, a problem related to the RC load concerns also the moment of switching of the capacitive load. If the capacitor to be turned on has a voltage other than the instantaneous v_{cm} , a current spike will occur during turn-on. For this reason, capacitor switching must occur whenever the instantaneous v_{cm} is at a fixed value. A solution is to perform the switching when the value of the common mode voltage is at its maximum value. At this instant, the capacitor current crosses zero, allowing the triacs turn off.

To further reduce the peaks of current due to these problems, low-pass filters may be inserted at the input of the loads. Ideally, these filters must be designed so that they do not significantly interfere in the RC load resistance and capacitance.

V. SIMULATION RESULTS

In order to validate the proposed topology for the RC load, simulations were performed on software PSIM. The simulated circuits are shown in Fig. 6. The value of R was chosen to conduct 400 mA when the inverter input voltage (v_{pv}) is 200 V, and the mains rms voltage is 220 V, 60 Hz. The value of C was also chosen to conduct 400 mA at the same condition. The chosen R and C values are 100 k Ω and 39 nF. The filter at the input of the resistive load is an RC filter (10 Ω , 1 nF). At the input of the capacitive load, a 100 Ω resistor was used as filter.

In the simulation of the resistive load (Fig. 6(a)), a 100 V dc voltage is added to a sinusoidal voltage of 155 V peak @ 60

Hz, as (3), simulating the condition described above. To validate the load switching, a signal varying from 0 to 255 was converted to 8-bits binary values, resulting on the MOSFET switching signals.

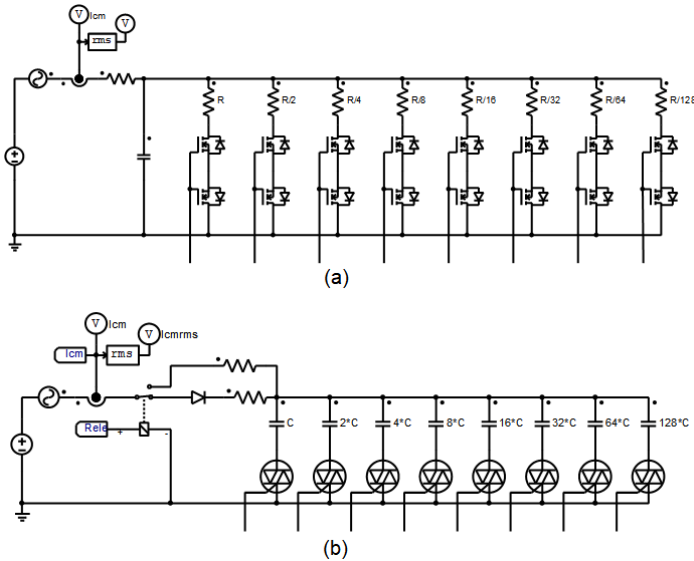


Fig. 6. Circuits simulated on PSIM: (a) Resistive load, (b) Capacitive load.

The simulation of the capacitive load (Fig. 6(b)) starts with the relay on its initial position, with all the triacs switched on. This way, all the capacitors are charged, through a diode and a resistor, with the peak value of the common mode voltage. After 5 seconds, the relay contact is switched, starting the normal operation of the capacitive load. The switching of the triacs occurs when the current through the load crosses zero, at the positive peak of v_{cm} .

The simulation results for the leakage current through the

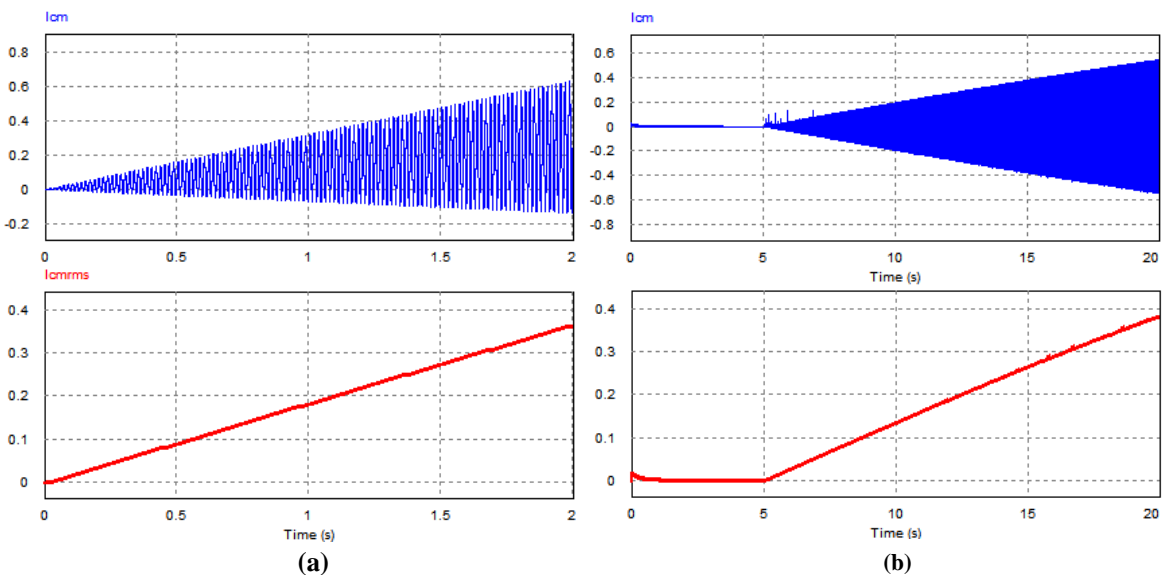


Fig. 7. Simulation of the current through the loads (Blue: Current value. Red: Current's RMS value.): (a) Resistive load, (b) Capacitive load.

loads are shown in Fig. 7. The resistive load circuit was simulated using ideal MOSFETs, so the turn-on and turn-off times of the switches are the same. Therefore it is not possible to visualize current spikes.

To simulate the capacitive load, the parasitic resistance of the triacs, during their open state, was considered. This resistance partially discharges the capacitors during the open state of the switches. All the triacs are switched at maximum input voltage. At this moment, a peak of current occurs in order to charge the capacitors that are being switched on. In Fig. 8(a), these peaks of current are shown. In Fig. 8(b), the voltage across one of the capacitors is shown. One can observe the voltage difference on the capacitor at the moment it is switched on, which results in a current spike. It is noted that the current spikes does not significantly change the rms value of the current through the load. Thus, this load is suitable for the IEC 62109-2 standard tests.

VI. CONCLUSION

Leakage current is an important issue concerning safety of photovoltaic inverters. This manuscript presented the requirements of the IEC 62109-2 standard, related to the protections against leakage current in photovoltaic inverters, and testing procedures to verify inverter compliance. A variable RC load suitable for the test has been proposed. Through simulations, it has been shown that this solution presents some problems related to current spikes, which can be solved using electronic circuits in combination with switching strategies.

The variable RC load is one of the parts of the leakage current test system, which will also be composed of a control system for the load, a current measuring system and a supervisory system to be developed. The complete system will be able to test inverters according to IEC 62109-2 in a photovoltaic inverter test laboratory.

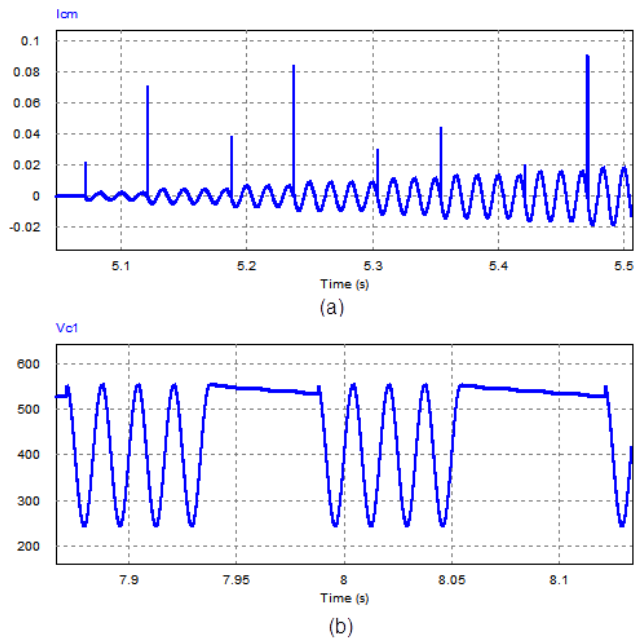


Fig. 8. Capacitive load simulation: (a) Peaks of current. (b) Voltage in one of the capacitors.

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