A HYBRID DIGITAL CONTROL METHOD FOR SYNCHRONOUS BUCK CONVERTERS USING MULTISAMPLED LINEAR PID AND V² CONSTANT ON-TIME CONTROLLERS

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***Abstract* – This paper presents a hybrid digital control method for a point-of-load (POL) synchronous buck converter. Two different controllers are used, seeking out to join good characteristics while eliminating drawbacks under different load conditions. For light loads, a constant on-time (COT) pulse frequency modulation (PFM) controller is used, in order to reduce power losses. For high loads, a linear pulse width modulation (PWM) PID controller is applied due to its better stability, with improved transitory response achieved by multisampling. The study was carried out for a step-down power converter from 3.3V to 1.2V with a maximum load current of 5A and the controller implemented in a Digital Signal Processor, DSP device. The feasibility of the proposed control method is shown with simulation and experimental results.**

***Keywords* – Buck synchronous, Control, Constant on-time, Multisampled, Point-of-load.**

NOMENCLATURE

D	Duty cycle.
M	Converter gain.
V_o	Output voltage.
V_i	Input voltage.
I_o	Output current.
I_L	Inductor current.
f_s	Switching frequency.
T_s	Switching period.
T_{on}	On-time for the high-side switch.
L	Converter inductance.
C	Converter capacitance.
R_L	Load resistance.

I. INTRODUCTION

Provided by the advances in integrated circuits (ICs), with the reduction of transistors size electronic devices are incorporating new elements, aiming to perform more functions, and consequently processing more power [1]. This improvement in ICs demands sharp requirements from power converters to properly supply them [2].

An electronic system consists of multiple loads and the supply requirements may vary for each one [2], in order to accommodate several power levels and the stringent requirements, some of these loads are supplied by point-of-load (POL) converters [3], which are converters close to the load and specifically designed to meet the load power requirements.

Some general aspects are important for the POL converter. One important characteristic is a fast response for load step, caused by the electronic nature of the loads. Another important feature is high efficiency, mainly at light load situation since the loads may spend long times in an idle state [1]-[2].

In terms of topology, the synchronous buck converter is the most suitable for such application. The low supply voltage needed justifies the step-down converter and the use of a low-side switch instead of a diode, which provides low on-state losses.

Ripple-based approaches are widely used to control POL converters. These types of control are well-known for their fast-transient response when compared to linear control approaches. In this scope, the constant on-time control method stands out because of its excellent light load efficiency [4].

Nowadays, most of POL control is still analog implemented, this occurs because high switching frequencies are used and the delays related with digital approaches may lead to instability problems [4]-[6]. The effort to solve the instability problems in digital schemes may jeopardize the fast transient responses when compared to those obtained with analog schemes. However, digital control provides some advantages, like the use of more sophisticated control structures, as well as providing easy adjustments and tuning [4]. In addition, as microchips are improving in processing power and getting cheaper, it is becoming worthwhile to explore digital solutions.

Several proposals have been presented trying to solve the problems related with digital control. One possible improvement is to use multisampling in linear control methods, reducing the phase delays and improving transitory responses [5]-[6]. Another possibility is to use compensation on constant on-time ripple based control [4].

This paper presents a digital control method, using a linear multisampled approach for high load conditions. On the other hand, for light load conditions, a digital constant on-time method is used. This choice permits to achieve a good transient response and stability in high load conditions and high efficiency at light load.

II. CONVERTER TOPOLOGY ANALISYS

The synchronous buck converter, Figure 1, is a step-down topology comprised by two MOSFETs (S1 - high-side, S2 - low-side) with an inductor and a capacitor working as the output filter. For low voltage applications, the use of a MOSFET instead of a diode, to assure the freewheeling stage, is beneficial in terms of efficiency, as the diode

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forward voltage is relatively higher than the MOSFET on-state voltage drop, causing a significant improvement on the converter losses.

Although this converter operation is similar to that of the standard buck, the controlled low-side switch introduces some differences. The current in the inductor may assume negative values, so to attain DCM (Discontinuous Current Mode) operation the gate signal of the low-side MOSFET must be controlled to inhibit the conduction as the inductor current reaches to zero. However, for CCM (Continuous Current Mode) this is not required.

Figure 2 shows the inductor current for CCM and DCM operation. It can be observed that there are three possible conduction stages: high-side switch conduction, low-side switch conduction and both switches open, respectively represented on the figure by the numbers 1, 2 and 3.

A. Operation modes and modulation

The pulse width modulation (PWM) is the most used method to drive static converters, in this modulation the duty cycle represents the relation between the on-time of S1 and the switching period.

$$D = \frac{T_{ON}}{T_s} = T_{ON} \times f_s \tag{1}$$

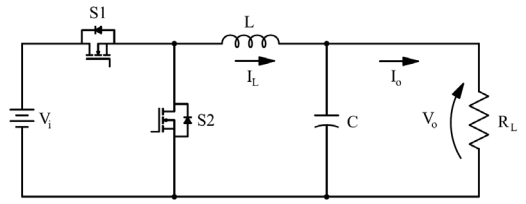

Fig. 1. Synchronous buck converter.

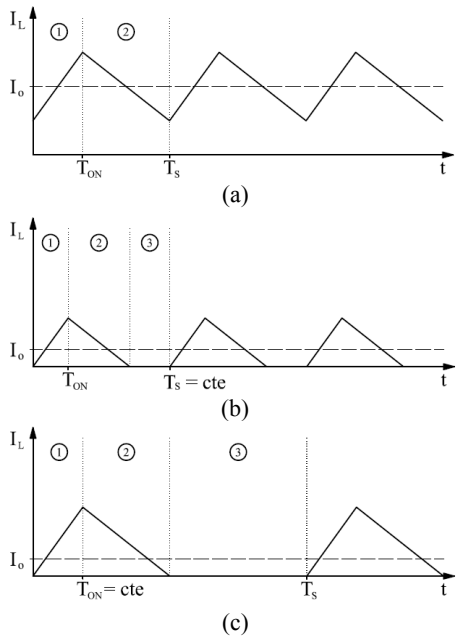

Fig. 2. Operation Modes. (a) CMM operation for PFM and PWM. (b) DCM operation for PWM. (c) DCM operation for PFM.

For a lossless buck converter, the duty cycle can be calculated as following, for a voltage gain M.

$$D_{CCM} = M \tag{2}$$

$$D_{DCM} = M\sqrt{\frac{I_o}{I_B}} \tag{3}$$

where I_B is the boundary current between CCM e DCM (critical current).

It can be seen that in CCM operation the duty cycle depends only of the voltage gain (M), meanwhile on DCM operation the duty cycle also depends on the load current.

On the other hand, constant on-time pulse frequency modulation (PFM) has a different approach, a constant on-time is defined for the high-side switch, and the frequency varies to create the modulation.

$$f_{sCCM} = \frac{M}{T_{ON_C}} \tag{4}$$

$$f_{sDCM} = \frac{M \times I_o}{T_{ON_C} \times I_B} \tag{5}$$

It can be seen that in CCM the frequency is constant but in DCM the frequency goes down with the load current.

Figure 2 shows the waveforms for PWM and PFM in both CCM and DCM operations. Thus, the main differences in operating frequency and inductor current can be viewed. The same behavior is expected for CCM operation, represented in Fig. 2(a), as the frequency is constant for both modulation. For DCM operation, observed in Fig. 2(b) for PWM and Fig. 2(c) for PFM, a difference in switching frequency is observed, remaining constant in PWM and reducing in PFM.

B. Efficiency Analysis

The electronic loads supplied by POL converters may have a wide range of output current from idle state to a full power operation [2]. The efficiency in all range of output power is a very important subject, especially at light loads [7], as the idle state may extend for long time intervals. It is important to understand the behavior of the losses mechanism to correctly design the converter and controller, aiming to minimize them.

The losses in converters can be divided in two groups: switching losses and conduction losses [7]-[8].

Switching losses are associated with the state transition of active elements, they occur as a result of charge and discharge of intrinsic capacitors of the MOSFETs as well as overlapping of current and voltage waveforms. The switching frequency plays an important role on reducing these losses since it is direct related to the number of switching. Voltage and current at the transition time are also relevant to switching losses, in that aspect DCM operation brings some advantages with half of the transitions occurring at zero current [7].

The conduction losses happen due to Joule effect in intrinsic resistances on the elements of the circuit. Reduce current ripple will have some impact reducing the RMS current, so CCM operation and higher inductances are better. Besides that, there is not much to do about these losses, except choosing the right elements to minimize them, this justify the low-side MOSFET over the conventional diode.

At light load situation, current is low, as well as conduction losses, thus switching losses plays a more important role on total losses. As the load goes up conduction losses increase in a higher rate than switching losses, therefore, at high loads, the conduction losses are more prominent.

The estimated efficiency (η) for PWM and PFM operating modes are described as follows.

$$\eta = \frac{P_{in}}{P_{out}} = \frac{P_{out} + P_{loss}}{P_{out}} \tag{6}$$

$$\begin{aligned} P_{loss} = {} & P_{S1c} + P_{S1on} + P_{S1off} + P_{S1gd} + \\ & P_{S2c} + P_{S2on} + P_{S2off} + P_{S2gd} + \\ & P_{Dc} + P_{Drr} + P_{Lc} + P_{Cc} \end{aligned} \tag{7}$$

where P_{S1c} and P_{S2c} are conduction loss, P_{S1on} and P_{S2on} are turn on losses, P_{S1off} and P_{S2off} are turn off losses, P_{S1gd} and P_{S2gd} are gate drive losses, all for MOSFETs S1 and S2. P_{Dc} and P_{Drr} are conduction and reverse recovery losses for the intrinsic diode of S2. P_{Lc} and P_{Cc} are conduction losses respectively for the inductor and capacitor.

These loss mechanisms are presented in detail with the equations on [7]-[8]. Parameters used for the efficiency estimative are shown on Table I. The duty cycle for PWM and switching frequency for PFM are approximated, for each load, using equations (2)-(5). Figure 3 presents the estimated efficiency results for the referred system, where a significant improvement is seen for PFM in DCM operation, while for CCM the are no difference in efficiency.

TABLE I
Parameters used for loss analysis

Parameter	Symbol	Value
Specification		
Input voltage	V_i	3.3V
Output voltage	V_o	1.2V
CCM switching frequency	f_s	100kHz
Voltage ripple	V_r	0.02% (24mV)
Inductor (SRP1265A)		
Inductance	L	4.7µH
DC resistance	DCR	7mΩ
CCM Current ripple	ΔI	2A
Boundary Current	I_b	1A
Capacitor (3x AMK325ABJ227MM-T)		
Capacitance	C	3x220µF
Equivalent series resistance	ESR	2mΩ
Dual Switch (IRF7910)		
On resistance	$R_{DS(on)}$	11.5mΩ
Turn-on delay time	$t_{d(on)}$	9.4ms
Turn-off delay time	$t_{d(off)}$	16ms
Total gate charge	Q_g	17nC
Diode forward voltage	V_{SD}	0.85V
Reverse recovery charge	Q_{rr}	60nC
Gate to source voltage	V_{GS}	5V

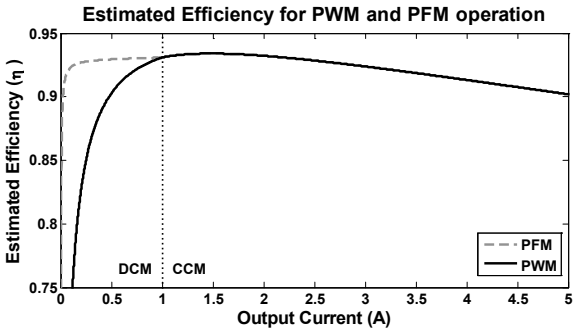

Fig. 3. Estimated efficiency for PWM and PFM operation.

III. PROPOSED HYBRID CONTROL

From the losses analysis it is clear that a PFM is necessary to maximize efficiency at light loads in DCM operation. The constant on-time control is a well know ripple-based controller to achieve this modulation [4].

For ripple to be used in digital control the acquisition frequency must be higher than the maximum switching frequency, otherwise the ripple would not be detectable by the control system. A higher number of acquisitions in the switching period achieves better results, while a low number of acquisitions may cause some oscillation, and instability problems [4] and [9].

It has been shown, Figure 3, that in CCM operation, both modulations have the same efficiency curve, as the frequency in PFM and PWM are constant. Thus, a linear PWM approach can be used to control in CCM mode without losing efficiency. The multiple samples already used for the ripple-based control can also be used in the linear control to improve transitory responses [5]-[6].

A. V^2 constant on-time control

The principle of operation of this control is to use the comparison of output voltage (V_O) with a reference (V_C), Figure 4. When the output voltage is lower than the reference a constant on-time pulse is generated that makes the output voltage goes up, as the pulse ends the voltage starts to go down until a next pulse is generated by the comparator.

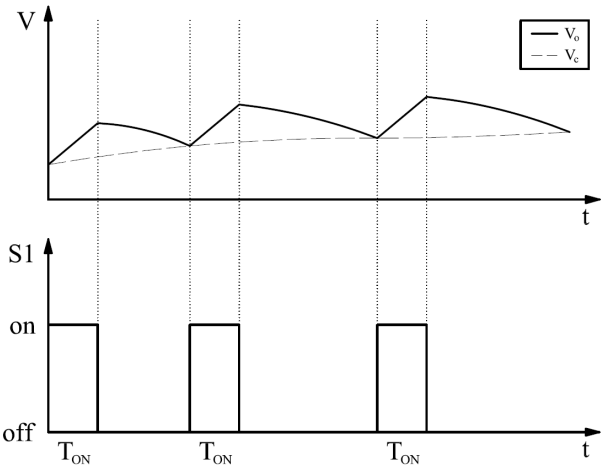

Fig. 4. Operation principle constant on-time control.

The reference (V_C) can be a constant value, but the ripple variation with the load may cause some small steady state errors. To solve this, one error compensator with integration is used, assuring null steady state error. The control block diagram with the compensator can be seen in Figure 5.

In digital systems there are a limited number of samples in each period, in this case, even if V_o is lower than the reference a new pulse will not occur until a new acquisition, hence, a low number of acquisition may cause oscillation problems as well as instability. This behavior is shown in Figure 6, in that case, two different switching periods are observed T_1 and T_2, caused by the delay (Δt) from the instant that V_C overcomes V_O until a sample is produced.

Using the constant on-time only for DCM is an excellent way to eliminate the drawbacks from this control, as it is stable [10] eliminating the need of compensation. In addition, the switching frequency goes down with the load, therefore, more samples are then made in a switching period mitigating the oscillation problem.

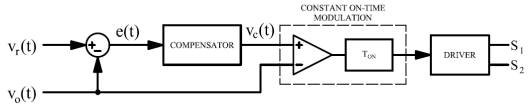

Fig. 5. Block diagram for constant on-time control.

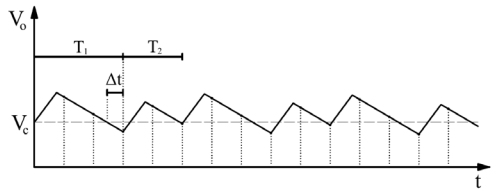

Fig. 6. Oscillation on digital constant on-time control.

B. Linear Control

The linear control is used to solve the problems verified on the digital implementation of the constant on-time control, for higher load current values in CCM operation. The controller acts over the duty cycle of the system, computing a modulation signal using the voltage error and a compensator, this signal is compared with a carrier signal (sawtooth waveform) on the desired frequency, generating the PWM signal. The block diagram can be seen in the Figure 7.

The compensator design uses the model of the converter relating the output voltage with duty cycle, given by:

$$G_{v_o d} = \frac{(V_i/LC)}{s^2 + (1/R_L C)s + (1/LC)} \tag{8}$$

For digital controllers there are delays inserted to the system from acquisition times, processing delays and digital PWM. This must be accounted for in the system model and impair the transitory response. Multisampling minimizes those delays and improves transitory responses even for low number of samples [5]-[6].

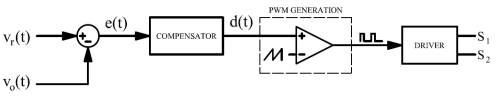

Fig. 7. Block diagram for linear control.

IV. CONTROLER DESIGN

The specifications of the converter are presented in Table II. The transition from DCM to CCM was defined at 20% of the nominal load, for good efficiency results, using this value to design the filter inductor. The filter capacitance value was defined to achieve voltage ripple requirements for all load range. The control was implemented using a DSP with a sample rate four times higher than the maximum switching frequency (CCM).

For the design of the linear compensator it was used the model of the buck converter (8), adding the delays inserted by the DPWM [5] and one sample period for processing time. The frequency response (bode) diagram for the complete model can be seen in Figure 8.

The crossover frequency of the system was set as one tenth of the switching frequency, i.e. 10 kHz, where the phase margin was -14 degrees. Due to the low phase margin a PID compensator was used resulting in the compensated system with phase margin of 40 degrees presented in the Figure 8. The designed PID transfer function is:

$$G_{PID} = \frac{4.524s^2 + 1.137\times10^5 s + 5.358\times10^8}{s^2 + 2.513\times10^5 s} \tag{9}$$

For the constant on-time control, T_{on} is selected as the same T_{on} for CCM in steady-state condition, from (4):

$$T_{ON} = \frac{M}{f_s} = \frac{0.3636}{100kHz} = 3.636\mu s \tag{10}$$

This choice provides the continuity during the shift from one controller to the other.

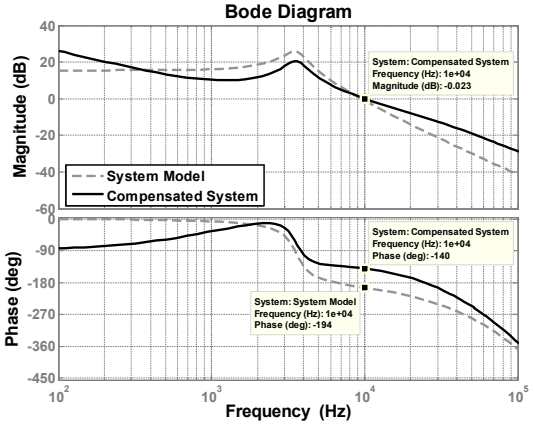

Fig. 8. Bode diagrams for CCM operation of the converter.

TABLE II
Converter Parameters

Parameter	Symbol	Value
Input Voltage	V_i	3.3V
Output Voltage	V_o	1.2V
Voltage Ripple	V_r	2% (24mV)
Output Current	I_o	0.05-5A
Switching Frequency	f_s	100kHz
Sampling Frequency	f_a	400kHz
Inductance	L	4.7µH
Capacitance	C	660µF

For the compensator, the objective is just to eliminate steady-state error caused by the ripple, so an integrator anti-windup was used, limiting the output between 1.1V and 1.3V, what is sufficient to correct this error.

In DCM operation is also needed to control the signal for the low-side switch, this can be done by approximating the low-side switch on-time (T_{on2}), which is possible knowing the input and output voltage as well as the on-time of the high-side switch.

$$T_{ON2} = \frac{T_{ON} \times (V_i - V_O)}{V_O} = 6.36\mu s \qquad (11)$$

A lower value is used to assure that the switch will be open before current gets to zero, leaving the final conduction for the intrinsic body diode. The impact on the losses is small, because at the time that the intrinsic diode is used the current is already very low. Using this approximation avoids the need for an analogic zero crossing detector circuit.

The selection of the control method is made by an average current sensor. Furthermore, a hysteresis band of 0.1A was applied for the boundary between modes to avoid multiple sequential mode changes.

Ultimately, for transitory moments it is forced the linear control until voltage stabilization, where, if it is the case, the constant on-time mode starts. This choice was made to achieve better transitory results, mainly on load reduction, where constant on-time mode can be very slow.

V. SIMULATION AND EXPERIMENTAL RESULTS

Prior to the laboratory prototype implementation, some simulation tests were made to verify the controller behavior and its performance against the specification for load transitory and comparative purposes with laboratory prototype results. For approximated results the simulation considered ADC resolution and sampling rate, DPWM resolution and DSP processing delay of one sample period.

The operation of the linear controller was tested for two load step changings, using as step set points the minimum and maximum load current in which this controller is designed. Figure 9 shows stable simulations results with some oscillation, overshoot of 150mV (12.5%) and a settling time of about 200ms.

The second simulation, presented in Figure 10, shows the constant on-time controller in steady state operation on different load conditions. It is verified the decreasing switching frequency and a small increase on voltage ripple with the reduction of the load in PFM mode. Figure 10 also shows a subharmonic oscillation, presented in the controller analysis, for high switching frequency caused by the relative small sample rate.

The transition between controllers was also tested in simulation with load variation using the smaller and higher load conditions for the converter. Figure 11 presents the controller behavior, where the linear control is selected in the transitory, as designed, before the transition to the constant on-time controller.

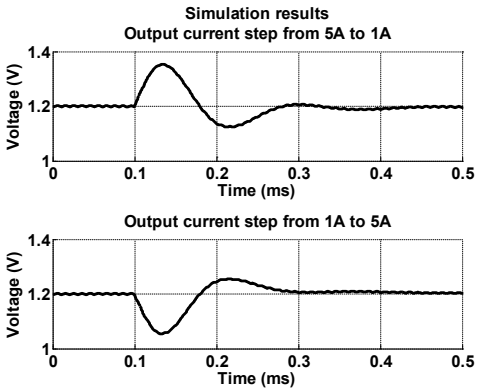

Fig. 9. Simulation results for output load step for linear controller.

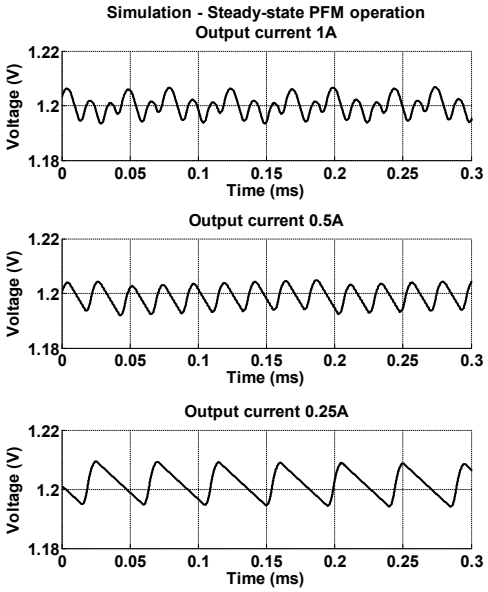

Fig. 10. Steady-state operation of PFM controller

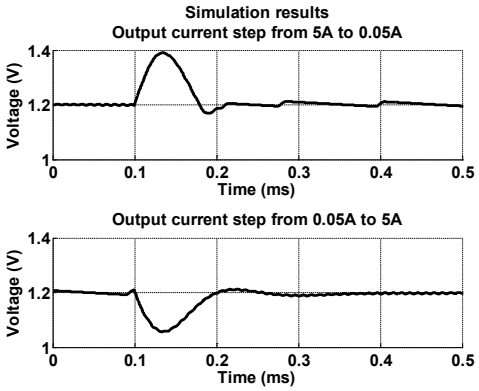

Fig. 11. Simulation results with transition between controllers.

With properly simulation results obtained, an experimental setup was assembled for preliminary tests, containing a DSP developer board and the designed board with converter, sensors and controllable load, Figure 12. The converter was supplied by a controllable voltage source, and a digital oscilloscope was used for measurements, saving the voltage waveform data to compare with simulations.

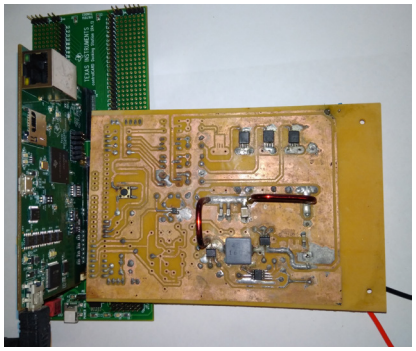

Fig. 12. Experimental setup with DSP and designed circuit.

Figure 13 compares simulation with experimental results for load steps. The experiment resulted on a less oscillatory response, attributed to a higher damping rate caused by non-ideal components, achieving better results than simulation.

The PFM operation was also tested for load steps in its range of operation, Figure 14. With the load step at 0.1ms it is verified the change in switching frequency with a fast transition expected from a ripple based control. The oscillation is higher than simulation, what can be caused by noise, but stay in range of designed ripple (2%).

The simulation and experimental results show the properly working of the system for the presented specifications. The controller provides fast transitory and stable response, as well as a good efficiency for light load operation.

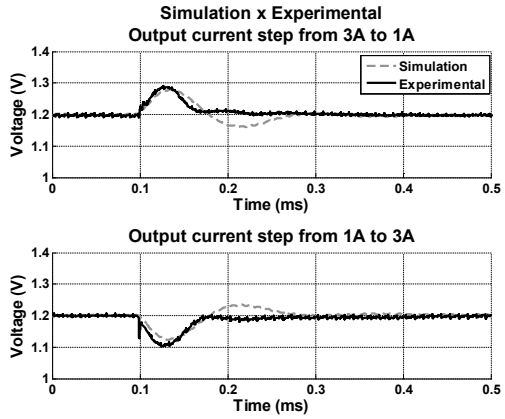

Fig. 13. Experimental results on linear control.

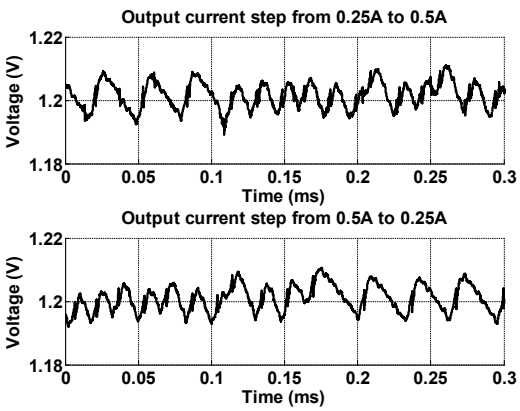

Fig. 14. Experimental results on constant on-time control.

VI. CONCLUSIONS

In this paper, a digital hybrid control method was proposed for synchronous buck converter. Operation and losses analysis were presented to justify the choices for the considered application.

By the use of PFM constant on-time control for DCM at light load situations and PWM linear multisampled for high loads it was possible to join good characteristics, mitigating the drawbacks of digital implementation. The results obtained in simulation and experiments achieved the objectives for the control system, proving the feasibility of the proposal.

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