Quadratic-Boost With Stacked Zeta Converter for High Voltage Gain Applications

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***Abstract*— This paper proposes a different approach to combine stacked and cascaded configuration of dc/dc pulse-width modulation converter cells in order to access the benefits of both structures in a single-stage topology with a single active switch. In addition to presenting and discussing the concepts of cascaded, stacked, and the combination of both, this paper also proposes a new topology derived from these concepts. It provides high voltage conversion ratio with improved efficiency. As the name implies, this converter is obtained from the combination of two well-known dc/dc converter circuits, the Isolated Zeta Converter and the Quadratic-Boost Converter. Hence, it presents the combined features of both, i.e., high step-up voltage conversion, low input current ripple (Quadratic Boost features), and low output current ripple (Zeta's feature). In order to verify the feasibility and performance of the converter presented, two 250-W prototypes circuits have been implemented.**

***Index Terms*— Cascade converter, dc–dc converter, high-voltage gain, stacked converter.**

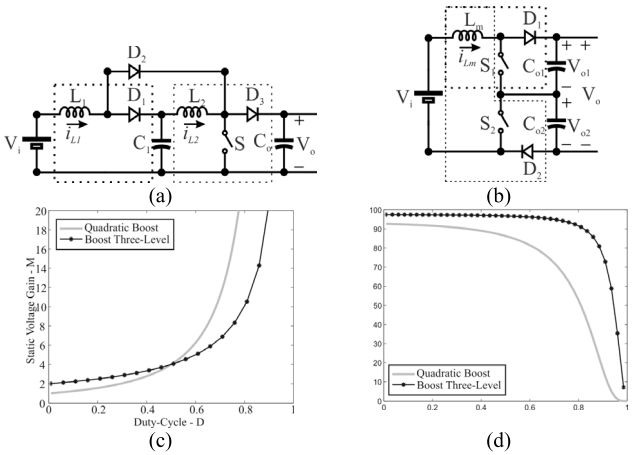

Fig. 1. Diagram of the possible connections for dc/dc PWM converter cells. (a) Quadratic boost converter circuit. (b) Double boost converter circuit. (c) Estimate theoretical voltage gain. (d) Estimate theoretical efficiency.

I. Introduction

In RECENT years, high step-up dc/dc converters have gained a great deal of interest mainly due to applications involving green energy system, such as wind energy, solar energy, and fuel cells [1], [2]. Typical 200–400 V dc bus application examples of high step-up dc/dc converters comprise dc distribution system [3], automotive application [4], battery charging system [5], led drives [6], and grid-connected inverters [7], [8]. In those applications, the voltage supplied by the source is commonly very low (typically 12–48 V) for direct application to a standard inverter to connect the green power to the grid. Hence, a step-up stage is usually employed between the renewable source and the grid inverter, forming a double-conversion topology. For low-power applications, the input voltage of the step-up stage is commonly a few dozen volts, demanding very high duty cycles to the converter switch. In this situation, the MOSFET equivalent series resistance (ESR) increases significantly and, summed up with inductor's and capacitor's ESR, causes a great deal in reducing the converter efficiency and even jeopardizing voltage gain and efficiency [9]–[11].

To overcome the aforementioned drawbacks, many alternatives to reduce conduction losses have been proposed, including the use of interleaved topologies in order to split the converter input current [12], [13], or to provide some kind of circuit modification to provide smaller duty-cycle levels such as the employment of voltage multipliers [12]–[14], switched inductors and/or capacitors [15], [16], and coupled inductors [17]–[19]. One of those techniques is the use of cascaded dc–dc converters; it is a simpler solution, since the voltage gain of each converter cell is multiplied by each other, yielding a large voltage gain [20], [21]. In order to avoid the need of several active switches, the integration of the power stages by means of the share of common components results in the so-called "Quadratic converters" [22], [23], for instance, the Quadratic Boost converter, Fig. 1(a). Unfortunately, such as the voltage gain, the efficiency of each step-up cell also multiplies by each other, reducing the overall efficiency. This situation may exacerbate by: 1) the high-current stresses of the first power stage and 2) the high-voltage stresses of the last stage, usually equal to the output voltage of the converter [24]. This latter feature aggravates the losses for MOSFET-based converters, since the ON resistance for this device is proportional to their breakdown voltage [25].

Alternatively to the cascaded converter cell association, the stacking of converter cells leads to the sum of their voltage gains, avoiding the multiplication, and consequent reduction of their efficiencies. The "Stacked two cells" of boost converters degenerates in the well-known three-level boost converter, Fig. 1(b). The stacked cells can double the voltage gain compared to the single converter cell [25], [26]. Regrettably,

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there are twice as many active switches, and the converter cost and complexity may increase.

From the above-mentioned context, it would be advantageous to achieve the benefits of both approaches, i.e., to combine the stacked and cascaded structures, keeping the high-voltage gain without penalizing the converter efficiency.

To achieve such goal, this paper proposes a different approach to arrange the dc/dc pulse-width modulation (PWM) converter cells, where the stack structure of two standard cells is combined with a cascaded cell (combination Type 1), or an cascade structure of two cells is combined with a stacked cell (combination Type 2).

In order to demonstrate the advantages of the proposed approach to generate high-voltage gain converters, an example of the combination between a Quadratic Boost and an Isolated Zeta Converter is presented and analyzed.

II. Single-Stage Topology Derivation

Based on the discussion of previous section, one can define two types of dc/dc PWM converter cells connections, the cascaded cell and the stacked cell structures, as shown in Fig. 2(a) and (b), respectively. In Fig. 2(a), the multicell converter consists of a set of "n" dc/dc PWM cells, namely, "cell 1," "cell 2," through "cell n," forming the cascaded configuration. Meanwhile, Fig. 2(b) converter consists of a set of "m" dc/dc PWM cells, namely, "cell a," "cell b," through "cell m," establishing the stacked configuration.

As can be seen in Fig. 2(a), the cascaded cell connection is characterized by the multiplication of the dc voltage gain of each cell, leading to a significant augment of the voltage conversion ratio of the topology—see (1). Regrettably, since the power flows in a single path from the source to the load, the full power is processed by each of the n cells, and consequently, the topology efficiency is the multiplication of the efficiency of each cell, as defined in (2). This means that the overall efficiency is smaller than any of the cells' efficiencies. In addition, it further reduces with the dc/dc PWM cell count

$$G_{\mathrm{VT(casc)}} = G_{V1} \times G_{V2} \times \cdots \times G_{Vn} \tag{1}$$

$$\eta_{T\,\mathrm{(casc)}} = \eta_1 \times \eta_2 \times \cdots \times \eta_n. \tag{2}$$

On the other hand, the stacked cell connection can be either additive or subtractive, depending on the polarity of the output voltage of each cell [27]. In the additive configuration, the topology is characterized by the sum of the dc voltage gain of each cell, leading to an augment of the voltage conversion ratio of the topology, see (3). Compared to the cascaded connection, the stacked topology dc voltage gain is smaller; however, since the power flows in separate paths through each dc/dc PWM cell, the overall efficiency is the average of all cell efficiencies (4). In other words, compared to the cascaded connection topology, efficiency is greater

$$G_{\mathrm{VT(stack)}} = G_{Va} + G_{Vb} + \cdots + G_{Vm} \tag{3}$$

$$\eta_{T\,\mathrm{(stack)}} = \frac{k_a\eta_a + k_b\eta_b + \cdots + k_m\eta_m}{m} \tag{4}$$

where $k_a + k_b + \cdots + k_m = 1$ and k_i $(i = a, b, \ldots, m)$ are the power sharing constant for each cells.

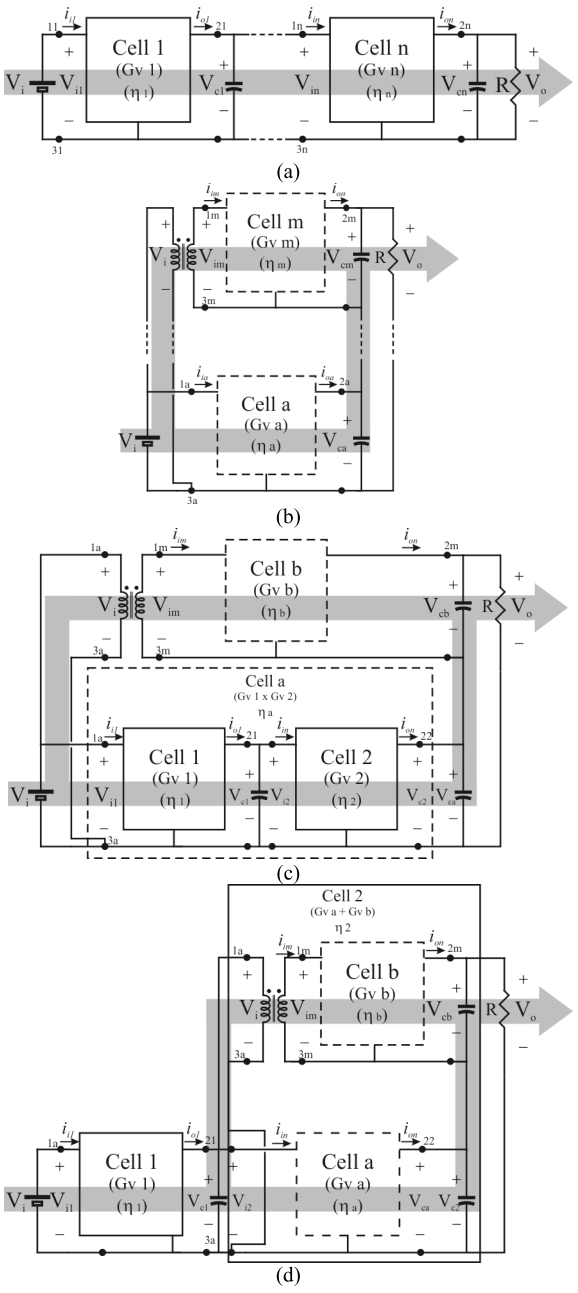

Fig. 2. Diagram of the possible connections for dc/dc PWM converter cells. (a) General cascaded cell connection. (b) General stacked cell connection. (c) Combination Type 1 (proposal). (d) Combination Type 2 (proposal).

Expression (5) summarizes the features of cascaded and stacked multicell structures. It becomes clear that cascaded configuration prevails for voltage gain and the stacked configuration for efficiency

$$G_{\mathrm{VT(stack)}} < G_{\mathrm{VT(casc)}}$$

$$\eta_{T\,\mathrm{(stack)}} > \eta_{T\,\mathrm{(casc)}}. \tag{5}$$

In order to achieve the benefits of both, Fig. 2(c) and (d) shows the circuit diagrams for three dc/dc PWM cells combinations. Fig. 2(c) shows the structure named combination Type 1; likewise, Fig. 2(d) shows the combination of Type 2. In Fig. 2(c), PWM "cell a" and "cell b" are stacked

$(GV_a + GV_b)$. Nevertheless, PWM "cell a" is already comprised by the cascade arrangement of PWM "cell 1" and "cell 2," $(G_{V1} \times G_{V2})$. Thus, the resulting topology presents the characteristics of both configurations, as can be seen in (6) and (7), for its dc voltage gain and efficiency, respectively

$$G_{\mathrm{VT(comb(Cas\_Stack))}} = (G_{V1} \times G_{V2}) + G_{Vb} \tag{6}$$

$$\eta_{T\,\mathrm{(comb(Cas\_Stack))}} = \frac{k_a(\eta_1 \times \eta_2) + k_b\eta_b}{2}. \tag{7}$$

By contrast, in Fig. 2(d), "cell 1" and "cell 2" are cascaded $(G_{Va} \times G_{Vb})$. As "cell 2" is already comprised by the stacked combination of "cell a" and "cell b," the resulting topology presents the characteristics of both configurations, as can be seen in (8) and (9), for its dc voltage gain and efficiency, respectively

$$G_{\mathrm{VT(comb(Stack\_Cas))}} = G_{V1} \times (G_{Va} + G_{Vb}) \tag{8}$$

$$\eta_{T\,\mathrm{(comb(Stack\_Cas))}} = \eta_1 \times \left(\frac{k_a\eta_a + k_b\eta_b}{2}\right). \tag{9}$$

Equations (6) and (8) show the static voltage gain for the Type 1 and 2 structures, respectively. Similarly, (7) and (9) define their theoretical efficiency.

In the following section the rules to merge the dc/dc PWM cell switches are discussed.

A. Type of DC/DC PWM Cell

In this section, the dc/dc converter cells, which will be combined, are defined and analyzed. In order to keep the analyses as concise and general as possible, the dc/dc converter cells are restrict to those that represent converters whose power flows only from the source to the load and make use of only one active switch. The general structure of such dc/dc PWM converter consists of three main parts: 1) the input voltage source (V_i); 2) the dc/dc PWM converter cell; and 3) the output voltage sink, which in turn consists of the parallel combination of load resistance (R) and output capacitor (C_o). It should be noted that the dc/dc PWM converter cell is defined as the circuit remaining when both, input source and output sink are removed. Thus, the dc/dc PWM converter cell may be defined as a topological combination of reactive elements and a pair of switches, one active (S_1) and one passive (D_1). For this paper, the dc/dc PWM cell is further split in "nonisolated cell" and "isolated cell," which also make use of an ideal transformer (turns-ratio N_2/N_1). Furthermore, for both PWM cells, the elements and the switches are arranged in such way that the duty cycle of the active switch has control of the output voltage (V_o).

The nonisolated dc/dc PWM converter cell in Fig. 3(a) is arranged as a three-terminal device, which can be connected in three different nonsymmetric possible ways to the input source and output sink (without connecting inductor L_2 and capacitor C_c) to generate three different converters, the buck, the boost, and the buck-boost topologies. These three topologies are the simplest ones since they make use of a single inductor (L_1). Adding the connections of inductor L_2 and buffer C_c, another three different circuits can be obtained, forming the Cúk, SEPIC, and zeta converters.

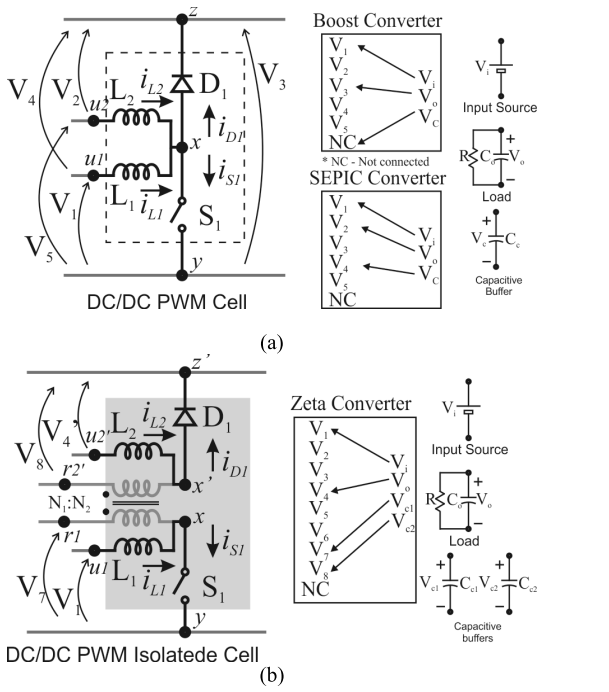

Fig. 3. Diagrams of the main parts of the dc/dc PWM converters. (a) Nonisolated converter cell, input voltage source (V_i), capacitive buffer (C), and output voltage sink (R, C_o). (b) Isolated converter cell, input voltage source, capacitive buffers (C_{c1}, C_{c2}), and output voltage sink (R, C_o).

These six topologies are considered as the standard dc/dc PWM converters and their relationship with its dc/dc PWM cells are summarized in Table I. In spite of the six nonisolated topologies, further analysis will concentrate the analysis only on the boost and buck-boost nonisolated converters.

If the nonisolated dc/dc PWM cell is to be replaced by the isolated one Fig. 3(b), a similar approach can be carried out, resulting in the forward and the flyback, as the simplest single-inductor topologies; and the isolated Cúk, SEPIC, and Zeta converters. These five topologies are considered as the standard isolated dc/dc PWM converters and their relationship with its dc/dc PWM cells are also summarized in Table I. Besides five isolated topologies, further analysis will take into account only flyback and Isolated Zeta converters.

Finally, one can observe that a cascaded or stacked connection, shown in Fig. 2, can be implemented by the combination of any two dc/dc PWM cells, shown in Fig. 3. Considering that each dc/dc PWM cell in the cascaded and/or stacked arrangement presents an active switch that controls its own duty cycle, this topology is known as a multistage converter.

B. Composite Switches and Cascaded DC/DC PWM Cells

The cascade combination of dc/dc PWM cells is quite simple and four examples for it are shown in Fig. 4. Main features for each configuration are summarized in Table II. It can be noted that, the Quadratic-Boost converter shows the higher voltage gain among the cascade two cells structures.

TABLE I

RELATIONSHIP OF THE ELEVEN STANDARD DC/DC CONVERTERS AND THEIR CONVERTER CELL TERMINALS

Conv. cell	V_i	V_o	C_{c1}	C_{c2}	Special Condition	Derived Topology
Non-isolated (Fig. 2(b))	z-y	z-u_1	---	---	Non	buck
	u_1-y	z-y	---	---	Non	boost
	u_1-y	z-u_1	---	---	Non	Buckboost
	u_1-y	z-u_2	z-y	---	Non	Cúk
	u_1-y	z-u_2	u_2-y	---	Non	SEPIC
	u_1-y	z-u_2	z-u_1	---	Non	Zeta
Isolated (Fig. 2(c))	r_1-y	z-u_2	---	---	V_8=V_{xy}	Forward
	u_1-y	z-r_2	---	---	V_7=V_1 (r_1-u_1)	Flyback
	u_1-y	z-u_2	r_1-y	z-r_2	Non	Isolated Cúk
	u_1-y	z-u_2	u_2'-y	---	L_2= L_2'/N	Isolated SEPIC
	u_1-y	z-u_2	z-r_2	---	V_7=V_1 (r_1-u_1)	Isolated Zeta

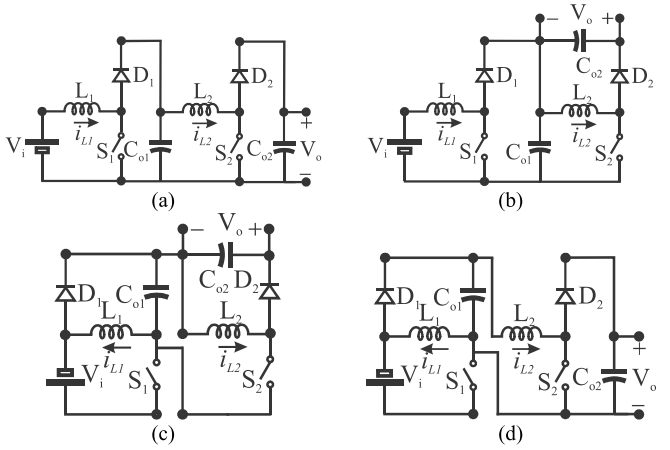

Fig. 4. Cascade two dc/dc PWM cells. (a) Boost^2 topology. (b) Boost-buck-boost topology. (ckboost^2 topology. (d) Buck-boost-boost topology.

TABLE II

SINGLE-STAGE CASCADED TWO DC/DC PWM CELL CONVERTER CHARACTERISTICS

Topology	Cell 1	Cell 2	Voltage Gain
Boost ^{2}	boost	boost	$\frac{V_o}{V_i}=\frac{1}{(1-D)^2}$
Buckboost ^{2}	buckboost	buckboost	$\frac{V_o}{V_i}=\frac{D^2}{(1-D)^2}$
Boost x buckboost	boost	buckboost	$\frac{V_o}{V_i}=\frac{D}{(1-D)^2}$
Buckboost x boost	buckboost	boost	

C. Input Section Integration and Stacked DC/DC PWM Cells

According to [28], the dc/dc PWM converters can be viewed as a three pieces (sections) circuit, where the converters that present the same or similar input sections can share it. The remaining middle and output sections can be arranged to provide the series or parallel combination of their output voltages. The extension of this concept is provided by exchanging one single-winding inductor of the standard topology by a coupled–inductor. The association rules defined in [24], and the combination of a nonisolated and an isolated dc/dc PWM converter cell the diagram are shown in Fig. 6. The combination of a nonisolated (dashed lines) [Fig. 3(a)] and isolated (gray square box) [Fig. 3(b)] dc/dc PWM converter cell is possible as long as they can share part of their components, Table III. It is evident that the common components must include the input voltage source and the active switch. It can also be seen that the magnetic coupling (transformer N_2/N_1) of the isolated dc/dc PWM cell is established by the replacement of the single-winding inductor L_1, by a coupled inductor.

To exemplify the concept of the input section sharing and dc/dc cell stacking, such concept is applied to three possible additive stacking configurations of a nonisolated dc/dc PWM cell of nonisolated (boost or buck-boost converter) and an isolated (Flyback or Zeta) dc/dc PWM cell, which are in stacked structures, Fig. 5.

TABLE III

REQUISITES FOR THE DC/DC PWM CELL STACKING

Requisite V_i	Requisite V_o	Special Condition	Topology
u_1 - y	z - any	---	boost (V_o: z-y)
			Cúk (V_o: z-u_{22})
			SEPIC (V_o: z-u_{22})
			buckboost (V_o: z-u_1)
			Zeta (V_o: z-u_2)
any - y	z'- any	V_8=V_{xy}	forward (V_i: r_1-y; V_o: z'-u_2')
		V_7= V_1	flyback (V_i: u_1-y;V_o: z'-r_2')
		---	Zeta (V_i: u_1-y; V_o: z'-u_2')

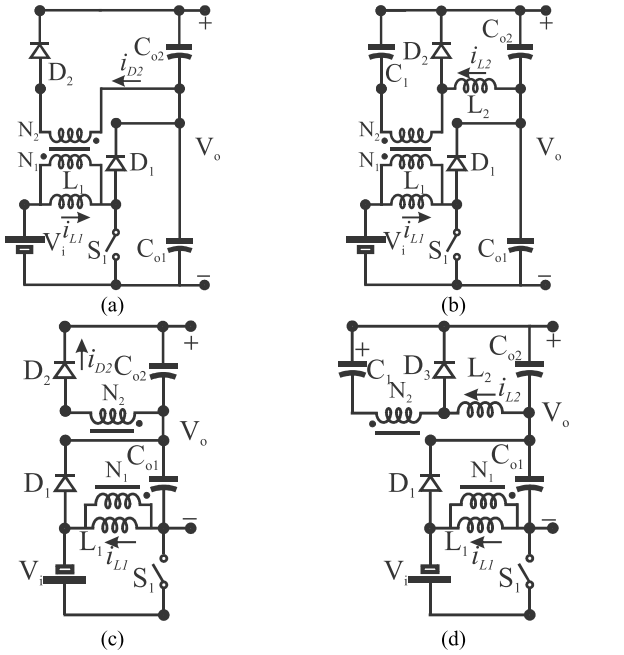

Fig. 5. Stacked two dc/dc PWM cells. (a) Boost-flyback topology. (b) Boost-zeta topology. (c) Buck-boost-flyback topology. (d) Buck-boost-zeta topology.

TABLE IV
SINGLE-STAGE STACKED TWO DC/DC PWM CELL CONVERTER CHARACTERISTICS

Topology	Cell a	Cell b	Voltage Gain
Boost-flyback	boost	flyback	$\frac{V_o}{V_i}=\frac{1+ND}{1-D}$
Boost-Zeta	boost	Zeta	
Buckboost -flyback	buckboost	flyback	$\frac{V_o}{V_i}=\frac{D(1+N)}{1-D}$
Buckboost -Zeta	buckboost	Zeta	

Fig. 5(a) shows the circuit of a boost-forward stacked converter. It can be seen that, the stacked converters share the input voltage (V_i), the inductor L_1, and the switch S_1. The demagnetizing of the transformer takes place at primary side, avoiding the need for a tertiary winding. Fig. 5(b) shows the circuit of a boost-Zeta stacked converter. Note that secondary sides for boost-flyback and boost-Zeta topologies are almost identical, differing just by replacing diode D_2 by capacitor C_1. This capacitor allows the demagnetizing of the transformer at the secondary side. Fig. 5(c) shows the circuit of buck-boost-flyback stacked converter. As can be seen, the secondary of the circuit has only the diode D_2 and the capacitor C_{o2}, and Fig. 5(d) illustrates the stacked buck-boost-flyback converter.

The stacked cell characteristics for these four converters are summarized in Table IV. It can be seen that the boost-Zeta converter is one of those with higher voltage gain. For this reason, this stacked cell configuration is selected to be further analyzed in the next sections.

D. Cascaded DC/DC PWM Cell Converters

Aiming to reduce the complexity and cost associated with control many switches, this section discusses the requirements to synchronize all switches in cascade configuration and to replace them than by a "combined switch." This can be done only when the switch operate in synchronism and shared a common node. Taking into account the ideal switch representation and its nodes as the switch pole (p) and the switch-throw (t), the possible combinations of two single switches (switch-throw and switch-throw—SPST), that can be replaced by a composite switch are shown in Fig. 7. It can be observed that the switches can be integrated and replaced by their corresponding "composite switch" subject to the following two constraints: 1) considering only ideal single-pole, single-throw devices, the switches must share at least a common node (com) and 2) when the switches (S_1 and S_2) are turned ON/OFF synchronously, the derived topology with the "composite switch" still behaves as its former dc/dc PWM converter cells operating individually. All switches that meet the above-mentioned conditions will belong to one of the four connection types shown in Fig. 6(a)–(d). Their "composite switches" counterparts designed as T-type composite switch (T-CS), inverted TSS, (IT-CS), Π-type composite switch (Π-CS), and inverted Π SS (I Π-CS) are shown in Fig. 6(e)–(h), respectively.

E. Cascaded and Stacked DC/DC PWM Cell Converters

Fig. 7 shows two similar diagrams representing the combination of cascading and stacking dc/dc PWM cells.

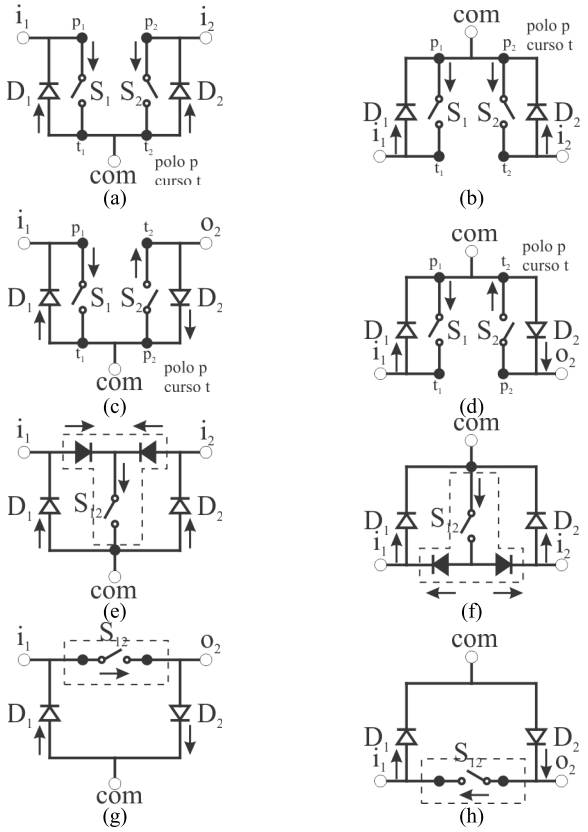

Fig. 6. Synchronous and composite switches. (a) Synchronous common throw. (b) Synchronous common pole. (c) Synchronous common throw-pole. (d) Synchronous common pole-throw. (e) Composite T-type. (f) Composite Inverse T-type. (g) Composite Π-type. (h) Composite inverse Π–type.

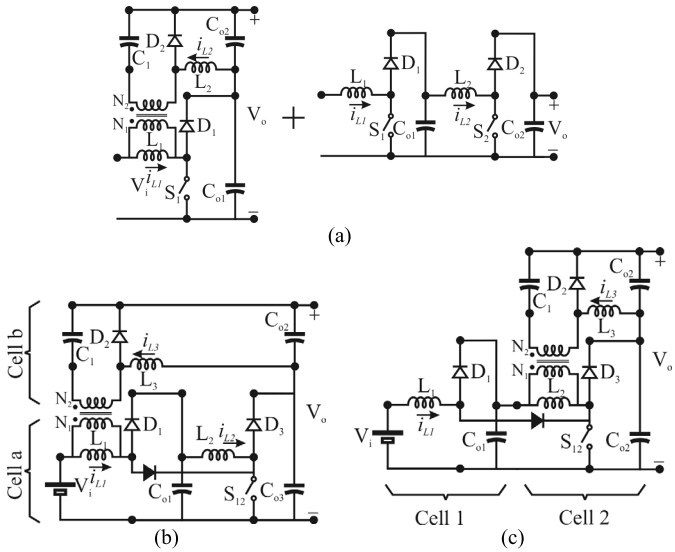

Fig. 7. DC/dc PWM cells combination. (a) Stacked and Cascade structure. (b) Combination Type 1. (c) Combination Type 2.

In Fig. 7(a), the stacking (boost zeta) is applied to the last of the cascaded cells (Quadratic Boost). Fig. 7(b) shows the Type 1 combination, and Fig. 7(c) shows the combination of the Type 2. Table V summarizes the possible combinations to yield the converters of Type 1. Similarly, Table VI summarizes

TABLE V
COMBINATION TYPE 1

Stacked			Statitc Voltage Gain
Cell a (Cascade)		Cell b	
Cell 1	Cell 2		
Boost	Boost	Flyback / Zeta	$M_1 = \frac{1+ND(1-D)}{(1-D)^2}$
Boost	Buckboost	Flyback / Zeta	$M_2 = \frac{D(1+N(1-D))}{(1-D)^2}$
Buckboost	Buckboost	Flyback / Zeta	$M_3 = \frac{D(D+N(1-D))}{(1-D)^2}$
Buckboost	Boost	Flyback / Zeta	$M_4 = \frac{D(1+N(1-D))}{(1-D)^2}$

TABLE VI
COMBINATION TYPE 2

Cascade			Static Voltage Gain
Cell 1	Cell 2 (Stacked)		
	Cell a	Cell b	
Boost	Boost	Flyback / Zeta	$M_5 = \frac{1+ND}{(1-D)^2}$
	Buckboost	Flyback / Zeta	$M_6 = \frac{D(1+N)}{(1-D)^2}$
Buckboost	Buckboost	Flyback / Zeta	$M_7 = \frac{D^2(1+N)}{(1-D)^2}$
	Boost	Flyback / Zeta	$M_8 = \frac{D(1+N)}{(1-D)^2}$

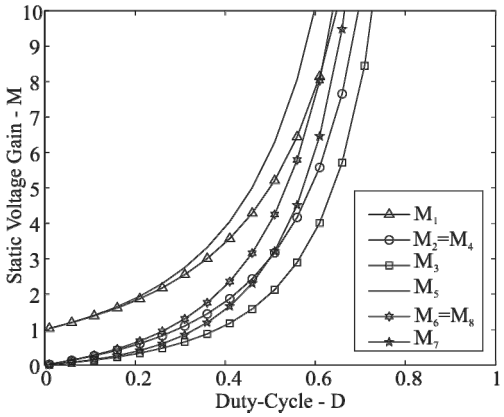

Fig. 8. Static Voltage Gain (M_i) versus duty cycle, where $N = 1$.

the possible combination to derive the combination of Type 2. Fig. 8 shows a comparison of the static voltage gain versus duty cycle, where N is equal to 1.

As can be seen in Fig. 8, the gain M_5 (Quadratic-Boost-Zeta converter Type 2) is higher when compared to the gain M_1 of the Quadratic-Boost-Zeta converter Type 1.

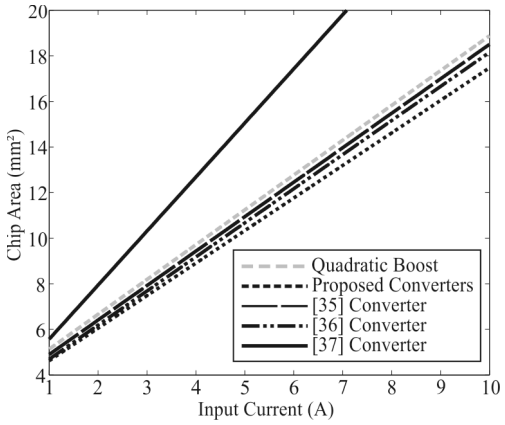

Fig. 9. Switch chip area as a function of the input current.

F. Comparative Evaluation

In order to clearly demonstrate the circuit advantages of the proposed converters, a detailed comparison is made in this section.

Table VII gives a comparison of seven converter topologies including the flyback converter, the forward converter, LLC converter [29], the current fed full-bridge converter [30], full-bridge converter [31], and the proposed converter Type 1 and 2 in terms of the number of components, for the same design specification. When the input and the output ripple of the converter are much higher, a large input and output filter is required. Thus, normally the capacitor used is of the electrolytic type. However, electrolytic capacitors are known to have a limited lifetime and are not compatible with the 20-year or longer lifetime that is desired for modern solar power systems. To increase the system lifetime, a high voltage film or similar capacitor for energy storage is preferred [32]. In this way, the proposed Type 1 and =2 converters have good reliability since the capacitors used are film type. The proposed Type 1 and 2 converters, flyback converter and forward converter have the lowest number of switches and gate drive which implies a lower system cost and lower complexity to generate the PWM signal. In other hand, the flyback converter has the lesser number of diodes. However the stress on this diode is high compared to other converters [33]. To achieve the same voltage gain ($M = 10$) and duty cycle ($D = 0.5$), the proposed Type 2 converter has the smaller turns ratio ($N = 2$). In [34], the flyback and forward converters for high-voltage gain applications, they present leakage problems and high voltage and current stress on their components which deteriorates the system efficiency. From this set of characteristics presented, the proposed Type 1 and 2 converters present in general the best characteristics for high voltage gain applications, in terms of reliability, cost, and simplicity.

Table VIII shows a comparison of the proposed converters with other high step-up converters that use similar methods to generate converters (cascaded and stacked). Table VIII summarizes the voltage gain, the voltage and current stresses of switch and the voltage stress of output diodes for the Quadratic Boost converter, the proposed Quadratic-Boost-Zeta Type 1 and 2 converters, quadratic boost with voltage

TABLE VII
COMPARISON OF SEVEN CONVERTER TOPOLOGIES AT $M = 10$, $V_i = 30$ V, $V_o = 240$ V, AND $D = 0.5$

Topology	Flyback	Forward	LLC converter [29]	Current Fed Full Bridge [30]	Full Bridge [31]	Proposed Converter Type 1	Proposed Converter Type 2
Number of switches	1	1	4	4	4	1	1
Number of Diodes	1	2	4	4	4	4	4
Number of capacitors	1	1	2	1	1	4	4
DC bus capacitors	Electrolytic capacitor	Electrolytic capacitor	Electrolytic capacitor	Electrolytic capacitor	Film Capacitor	Film Capacitor	Film Capacitor
Number of magnetics	1	2	1	2	2	3	3
Transformer Turns Ratio	8	16	16	8	16	4	2
Duty Cycle (D)	0 < D < 1	D < 0.5	0 < D < 1	0 < D < 1	0 < D < 1	0 < D < 1	0 < D < 1
Current Input Ripple	Large	Large	Large	Normal	Large	Normal	Normal
Current Output Ripple	Large	Normal	Large	Large	Normal	Normal	Normal
PWM Strategy	Easy	Easy	Complex	Complex	Complex	Easy	Easy
Number of Gate Drive	1	1	4	4	4	1	1
Cost	small	small	medium	medium	medium	small	small

TABLE VIII
COMPONENTS VOLTAGE AND CURRENT STRESSES

Description	Converters				
	Quadratic Boost	Proposed Type 1 and Type 2	[35]	[36]	[37]
Voltage Gain (M)	$\frac{1}{(1-D)^2}$	$\frac{ND+1}{(1-D)^2}$	$\frac{ND+1}{(1-D)^2}$	$\frac{N(3D+2)+(2-D)}{2(1-D)^2}$	$\frac{1+D}{(1-D)^2}$
Voltage Stress of Switch	$\frac{V_i}{(1-D)^2}$	$\frac{V_i}{(1-D)^2}$	$\frac{V_i}{(1-D)^2}$	$\frac{(2-D(N-1))V_i}{2(1-D)^2}$	$\frac{V_i}{(1-D)^2}$
Current Stress of Switch	$2I_i\sqrt{D}$	$\left(2+\frac{(1-D)^2}{ND+1}\right)\sqrt{D}I_i$	$\left(1+\frac{(1-D)^2}{ND+1}\right)2\sqrt{D}I_i$	$\left(1+\frac{2(1-D)^2}{N(3D+2)+(2-D)}\right)2\sqrt{D}I_i$	$\left(2\sqrt{D}+1\right)I_i$
Voltage Stress of Output Diodes	$\frac{V_i}{(1-D)^2}$	$\frac{V_i}{(1-D)^2}$	$\frac{NDV_i}{(1-D)^2}$	$\frac{NV_i}{(1-D)^2}$	$\frac{V_i}{(1-D)^2}$

TABLE IX
INPUT PARAMETERS

Symbol	Quadratic Boost Zeta Converter	
	Description	Value
P_i	Input Power	250 W
V_i	Input Voltage	30 V
V_o	Output Voltage	240 V
D	Duty Cycle	0.5
M	Static Voltage Gain	8
f_s	Switching Frequency	100 kHz

TABLE X
PROTOTYPE PARAMETERS

Symbol	Description	Quadratic Boost Zeta Converter Type 1	Quadratic Boost Zeta Converter Type 2
		Value	Value
N	Turns Ratio	4	2
L_1	Inductor L_1	95 µH	130.75 µH
L_2	Inductor L_2	7.8 mH	7.47 mH
L_3	Inductor L_3	261 µH	91.57 µH
C_{o1}	Capacitor C_{o1}	15.91 µF (film)	15.98 µF (film)
C_1	Capacitor C_1	3.5 µF (film)	3.5 µF (film)
C_{o2}	Capacitor C_{o2}	175 nF (film)	175 nF (film)
C_{o3}	Capacitor C_{o3}	15 µF (electrolytic)	7.96 µF (film)
S	Switch	IRFP260N (200 V/50 A)	IRFP260N (200 V/50 A)
D_1, D_3	Diode	MBR20200CT (200 V/20 A)	MBR20200CT (200 V/20 A)
D_2	Diode	STPSC4H065 (600 V/4 A)	STPSC4H065 (600 V/4 A)

multiplier converter [35], quadratic boost with switched capacitors converter [36], and Quadratic Boost converter with capacitor–inductor–diode [37]. From Table VIII, the voltage gain of proposed converter is not the higher. On the other hand, the voltage and current stresses of the switch S and voltage stress of output diodes of proposed converters are less than other converters shown in Table VIII. In general, these characteristics make it possible to use lower voltage diodes and switch, hence the conduction loss and switching loss could be reduced leading to efficiency improvement.

As can be seen, all converters shown in Table VIII have a single switch. For the same design specification (Table IX) of converters and the methodology presented in [38]–[40], it is possible to estimate the behavior of current stress with the chip area. It should be noted that, the equation used to calculate the chip area is linear [38]–[40], in this way Fig. 9 shows the behavior of the chip area of the switch by different input current of the converters shown in Table VIII. Fig. 9 shows that the chip area of the proposed converters is lower in relation to the other converters, so the current stress of the proposed converters is also lower.

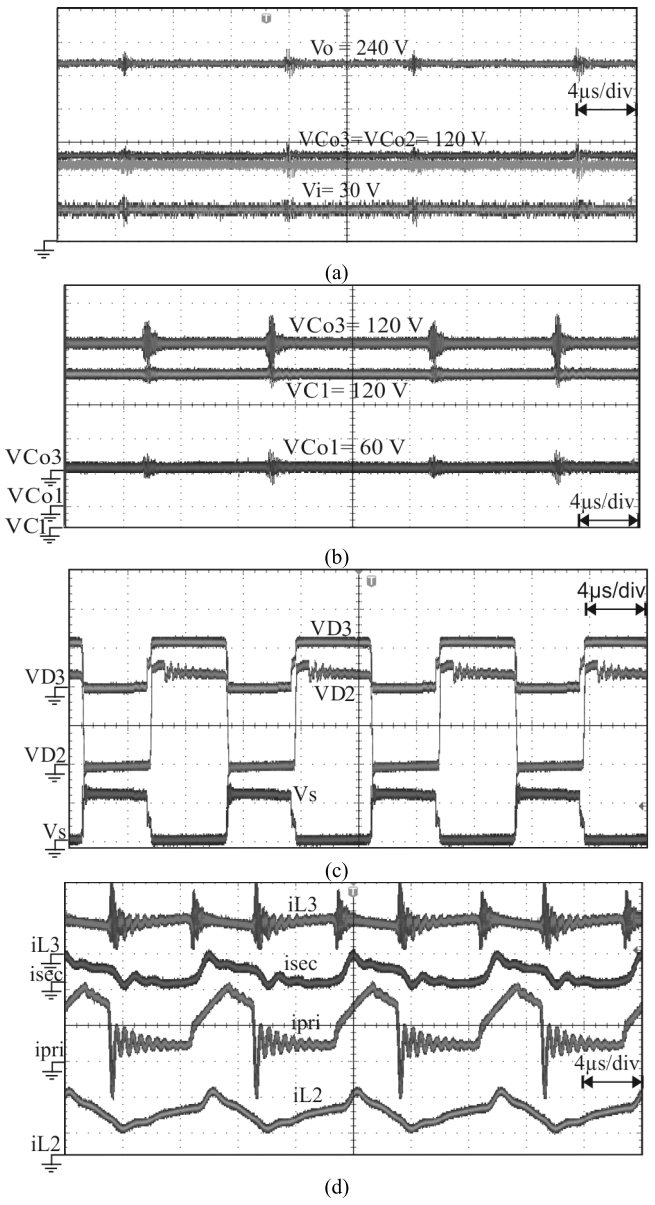

Fig. 10. Experimental results of Quadratic-Boost-Zeta converter Type 1. (a) Voltage waveforms V_o, V_{Co2}, V_{o3}, V_i. (b) Voltage waveforms V_{Co1}, V_{C2}, and V_{Co3}. (c) Voltage waveforms V_s, V_{D2}, and V_{D3b}. (d) Inductors current waveforms i_{L2}, $i_{\text{pri}} = i_{L1} + i_{N1}$, $i_{\text{sec}} = i_{N2}$, and i_{L3}.

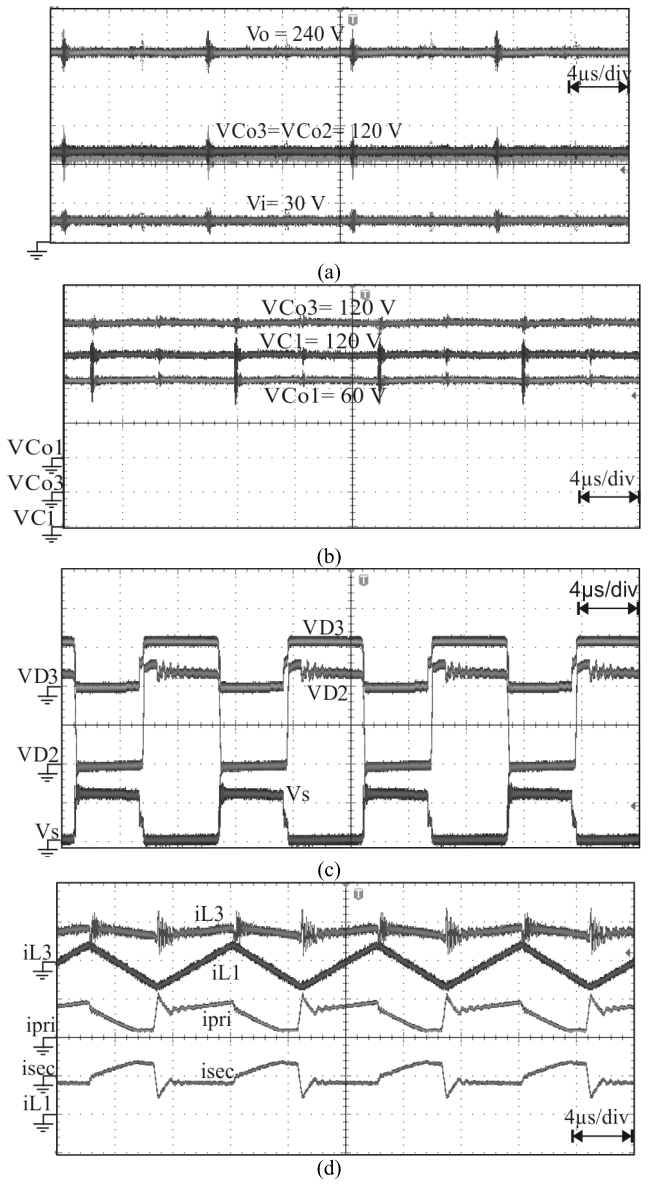

Fig. 11. Experimental results of Quadratic-Boost-Zeta converter Type 2. (a) Voltage waveforms V_o, V_{Co2}, V_{o3}, V_i. (b) Voltage waveforms V_{C1}, V_{Cz}, and V_{oz}. (c) Voltage waveforms V_s, V_{D2}, and V_{D3b}. (d) Inductors current waveforms i_{L1}, $i_{\text{pri}} = i_{L2} + i_{N1}$, $i_{\text{sec}} = i_{N2}$, and i_{L3}.

III. Experimental Evaluation

To confirm the theoretical analyses presented in the previous sections, two prototypes sample have been made for the Quadratic-Boost-Zeta converter Type 1 and Type 2, considering the following parameters given Table IX. Based on the parameters specified given in Table X, the key waveforms of the Quadratic-Boost-Zeta converter Type 1 and Type 2 are shown in Figs. 10 and 11, respectively. The input source is the Agilent E4360A; the load is the electronic load RBL488; the PWM generator is DSP TMS320F28335; measurement Equipment is the Tektronix Encore MD03000; and measurement Efficiency is Yokogawa WT1800.

Figs. 10(a) and 11(a) show the output voltage of the converter ($V_o = 240$ V) is eight times as high as the input voltage ($V_i = 30$ V); it is a result of the sum converters in cascaded and stacked cell combinations $V_{\text{Co3}} = 120$ V and $V_{\text{Co2}} = 120$ V. Figs. 10(b) and 11(b) show the association with the output voltage of the Quadratic-Boost section ($V_{\text{Co3}} = 120$ V), $V_{C1} = 120$ V and $V_{\text{Co1}} = 60$ V. Figs. 10(c) and 11(c) show the switch S voltage (V_s) where V_s is the same voltage of the output voltage of the cascade cell ($V_s = 120$ V); the diode D_2 voltage (V_{D2}), where V_{D2} is equal to 240 V, and the diode D_3 voltage (V_{D3}), where V_{Db} is equal to the output voltage of the Quadratic-Boost section ($V_{D3} = 120$ V). Figs. 10(d) and 11(d) show the inductor L_1 current (i_{L1} and i_{L2}), the current in the primary and secondary of the (i_{N1}), (i_{N2}), and current of the output inductor L_3 (i_{L3}).

Finally, Fig. 12 shows the experimental efficiency. Fig. 12 shows the efficiency of Quadratic-Boost-Zeta converter

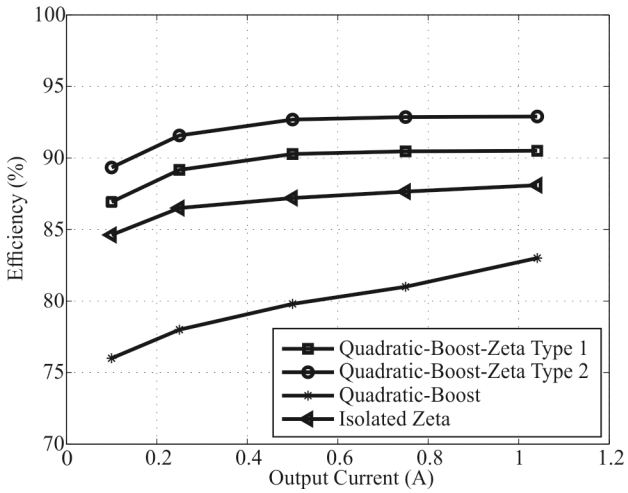

Fig. 12. Experimental efficiency of Isolated Zeta, Quadratic Boost And Quadratic-Boost-Zeta Type 1 and Type 2 converters for $V_o = 240$ V.

Type 1 and Type 2 prototypes, Quadratic boost converter prototype and Isolated Zeta converter prototype as a function of the output current. The static voltage gain equal to 8, it is evident that the efficiency of the Quadratic-Boost-Zeta converter Type 2 is higher than the other converters. It is important to note that experimental evaluation concentrates on supporting the theoretical results of voltage conversion ratio and potential step-up converters.

According (6) and (7), for the Quadratic-Boost-Zeta converter Type 1, the "cell 1" and "cell b" process 50% of the power, respectively. After the energy processing and the losses of "cell 1," "cell 2" processes the remaining power. It means that the Zeta cell contributes 50% efficiency. While, the efficiency of the input boost cell is multiplied by the efficiency of the second boost cell, thus contributing to the other 50% efficiency.

From (8) and (9), for the Quadratic-Boost-Zeta converter Type 2, the "cell 1" processes 100% of the power. After the energy processing and the losses of "cell 1," "cell a" and "cell b" processes 50% of the remaining power, both. It means that the input boost cell efficiency is multiplied by the efficiency of the second boost cell and Zeta cell, which process 50% of efficiency, each.

IV. Conclusion

This paper present an analysis of a high step-up dc/dc converter named Quadratic-Boost-Zeta converter. This converter is a combination of stacked and cascaded configuration of dc/dc PWM converter cells with the aim to achieve the advantages of both structures in a single-stage topology with a single active switch. This converter is based on the combination of three standard dc/dc converters, which are the Isolated Zeta converter and the tow boost converter. The static gain, the voltage and current stress of the components, analysis of operation, and design for one of the converter were shown. Experimental results of the Quadratic-Boost-Zeta converters Type 1 and Type 2 were provided

References

[1] F. L. Tofoli, D. de C. Pereira, W. J. de Paula, and D. de S. O. Júnior, "Survey on non-isolated high-voltage step-up DC–DC topologies based on the boost converter," *IET Power Electron.*, vol. 8, no. 10, pp. 2044–2057, 2015.

[2] L. Zhang, D. Xu, G. Shen, M. Chen, A. Ioinovici, and X. Wu, "A high step-up DC to DC converter under alternating phase shift control for fuel cell power system," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1694–1703, Mar. 2015.

[3] K.-C. Tseng, C.-C. Huang, and C.-A. Cheng, "A single-switch converter with high step-up gain and low diode voltage stress suitable for green power-source conversion," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 363–372, Jun. 2016.

[4] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.

[5] L. H. S. C. Barreto. P. P. Praca, D. S. Oliveira, Jr., and R. P. T. Bascope, "Single-stage topologies integrating battery charging, high voltage step-up and photovoltaic energy extraction capabilities," *Electron. Lett.*, vol. 47, no. 1, pp. 49–50, Jan. 2011.

[6] M. F. de Melo, W. D. Vizzotto, P. J. Quintana, A. L. Kirsten, M. A. D. Costa, and J. Garcia, "Bidirectional grid-tie flyback converter applied to distributed power generation and street lighting integrated system," *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 4709–4717, Nov./Dec. 2015.

[7] T.-F. Wu, C.-L. Kuo, L.-C. Lin, and Y.-K. Chen, "DC-bus voltage regulation for a DC distribution system with a single-phase bidirectional inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 210–220, Mar. 2016.

[8] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen, and I. Batarseh, "A single-stage microinverter without using eletrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2677–2687, Jun. 2013.

[9] E. Babaei and O. Abbasi, "Structure for multi-input multi-output DC–DC boost converter," *IET Power Electron.*, vol. 9, no. 1, pp. 9–19, 2016,

[10] C. Zhao, H. Yin, Z. Yang, and C. Ma, "Equivalent series resistance-based energy loss analysis of a battery semiactive hybrid energy storage system," *IEEE Trans. Energy Convers.*, vol. 30, no. 3, pp. 1081–1091, Sep. 2015.

[11] T. J. Liang and K. C. Tseng, "Analysis of integrated boost-flyback step-up converter," *Inst. Elect. Eng. Proc.-Electr. Power Appl.*, vol. 152, no. 2, pp. 217–225, Mar. 2005.

[12] W. Li, Y. Zhao, J. Wu, and X. He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 133–143, Jan. 2012.

[13] M. Muhammad, M. Armstrong, and M. A. Elgendy, "A nonisolated interleaved boost converter for high-voltage gain applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 352–362, Jun. 2016.

[14] L. Müller and J. W. Kimball, "High gain DC–DC converter based on the cockcroft–walton multiplier," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6405–6415, Sep. 2016.

[15] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2063–2072, Apr. 2015.

[16] K. W. E. Cheng and Y.-M. Ye, "Duality approach to the study of switched-inductor power converters and its higher-order variations," *IET Power Electron.*, vol. 8, no. 4, pp. 489–496, 2015.

[17] N. Vázquez, F. Medina, C. Hernández, J. Arau, and E. Vázquez, "Double tapped-inductor boost converter," *IET Power Electron.*, vol. 8, no. 5, pp. 831–840, 2015.

[18] S.-M. Chen, M.-L. Lao, Y.-H. Hsieh, T.-J. Liang, and K.-H. Chen, "A novel switched-coupled-inductor DC–DC step-up converter and its derivatives," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 309–314, Jan./Feb. 2015.

[19] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016.

[20] S. H. Chincholkar and C.-Y. Chan, "Investigation of current-mode controlled cascade boost converter systems: Dynamics and stability issues," *IET Power Electron.*, vol. 9, no. 5, pp. 911–920, 2016.

[21] D. Maksimovic and S. Cuk, "Switching converters with wide DC conversion range," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 151–157, Jan. 1991.

[22] N. Zhang, D. Sutanto, K. M. Muttaqi, B. Zhang, and D. Qiu, "High-voltage-gain quadratic boost converter with voltage multiplier," *IET Power Electron.*, vol. 8, no. 12, pp. 2511–2519, 2015.
[23] Y.-M. Ye and K. W. E. Cheng, "Quadratic boost converter with low buffer capacitor stress," *IET Power Electron.*, vol. 7, no. 5, pp. 1162–1170, 2014.
[24] S. Sathyan, H. M. Suryawanshi, M. S. Ballal, and A. B. Shitole, "Soft-switching DC–DC converter for distributed energy sources with high step-up voltage capability," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7039–7050, Nov. 2015.
[25] S. Dusmez, A. Hasanzadeh, and A. Khaligh, "Comparative analysis of bidirectional three-level DC–DC Converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3305–3315, May 2015.
[26] H.-C. Chen and W.-J. Lin, "MPPT and voltage balancing control with sensing only inductor current for photovoltaic-fed, three-level, boost-type converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 29–35, Jan. 2014.
[27] A. M. S. S. Andrade, L. Schuch, and M. L. de S. Martins, "High step-up PV module integrated converter for PV energy harvest in FREEDM systems," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1138–1148, Mar./Apr. 2017.
[28] A. M. S. S. Andrade, J. R. Dreher, and M. L. de S. Martins, "High step-up integrated DC–DC converters: Methodology of synthesis and analysis," in *Proc. Brazilian Power Electron. Conf.*, 2013, pp. 50–57.
[29] S. Abdel-Rahman, "Resonant LLC converter: Operation and design," Infineon Technol. North America (IFNA) Corp., Morgan Hill, CA, USA, Appl. Note AN 2012-09, Sep. 2012.
[30] M. Baei and G. Moschopoulos, "A ZVS-PWM full-bridge boost converter for applications needing high step-up voltage ratio," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, Feb. 2012, pp. 2213–2217.
[31] M. Uslu, "Analysis, design, and implementation of a 5 KW zero voltage switching phase-shifted full-bridge DC/DC converter based power supply for arc welding machines," M.S. thesis, Dept. Elect. Electron. Eng., Middle East Tech. Univ., Ankara, Turkey, Nov. 2012.
[32] Y. Levron, S. Canaday, and R. W. Erickson, "Bus voltage control with zero distortion and high bandwidth for single-phase solar inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 258–269, Jan. 2016.
[33] Q. Zhao, F. Tao, Y. Hu, and F. C. Lee, "Active-clamp DC/DC converters using magnetic switches," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, vol. 2. Anaheim, CA, USA, Mar. 2001, pp. 946–952.
[34] W.-J. Cha, Y.-W. Cho, J.-M. Kwon, and B.-H. Kwon, "Highly efficient microinverter with soft-switching step-up converter and single-switch-modulation inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3516–3523, Jun. 2015.
[35] S.-M. Chen, T.-J. Liang, L.-S. Yang, J.-F. Chen, and K.-C. Juang, "A quadratic high step-up DC–DC converter with voltage multiplier," in *Proc. IEEE Int. Elect. Mach. Drives Conf. (IEMDC)*, Niagara Falls, ON, Canada, May 2011, pp. 1025–1029.
[36] P. Saadat and K. Abbaszadeh, "A single-switch high step-up DC–DC converter based on quadratic boost," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7733–7742, Dec. 2016.
[37] P. Yang, J. Xu, G. Zhou, and S. Zhang, "A new quadratic boost converter with high voltage step-up ratio and reduced voltage stress," in *Proc. 7th Int. Power Elect. Motion Control Conf.*, Harbin, China, Jun. 2012, pp. 1164–1168.
[38] T. Friedli and J. W. Kolar, "A semiconductor area based assessment of AC motor drive converter topologies," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Washington, DC, USA, Feb. 2009, pp. 336–342.
[39] T. B. Soeiro and J. W. Kolar, "The new high-efficiency hybrid neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1919–1935, May 2013.
[40] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, Glendale, AZ, USA, Nov. 2010, pp. 391–396.

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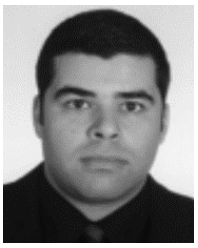

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