Comparative Evaluation of Single Switch High-Voltage Step-Up Topologies Based on Boost and Zeta PWM Cells

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***Abstract*—This paper presents a comparative evaluation of eight high-voltage step-up converters based on different associations of boost and zeta standard dc–dc pulse width modulation (PWM) cells. These eight converters present different characteristics such as cascaded and stacked PWM cell associations, as well as isolated winding coupled inductors, tapped winding coupled inductors, and noncoupled inductors. In order to explore the advantages and address the limitations of each topology, several comparative evaluations concerning static voltage gain, power losses, current and voltage stresses, component stress factors, power density, relative cost, and efficiency were carried out. From the theoretical analysis and experimental results, the association named stacked boost–zeta with autotransformer yielded the highest efficiency and power density and resulted in the most attractive converter for the case study.**

***Index Terms*—Boost converter (BC), dc/dc converter, high step-up, step-up, zeta converter (ZC).**

I. Introduction

INTEREST in dc–dc converters has been growing in recent years [1], [2], mainly for renewable energy applications such as those that make use of photovoltaic panels, fuel cells, and others with dc source characteristics [3]–[6]. In such applications, the voltage provided by the renewable source is often only a few dozen volts, and thus, it must be adjusted by a step-up power converter prior to being inverted by a standard pulse width modulation (PWM) H-bridge and injected into the ac grid [7]–[10].

Over the years, many dc–dc converters have been proposed in the literature. But, the standard dc–dc PWM converters that are capable of providing voltage step-up are the boost and the buck–boost. Other similar converters with buck–boost characteristics are the Cuk, SEPIC, and zeta converters (ZCs). Any of these converters can, ideally, achieve high-voltage levels by increasing their switch duty cycle. Unfortunately, when the duty cycle approaches unity, converter efficiency and voltage gain degrade noticeably, mainly due to the increased rms current through the components and the increase of the ON-state resistance of the MOSFET switch [11], [12].

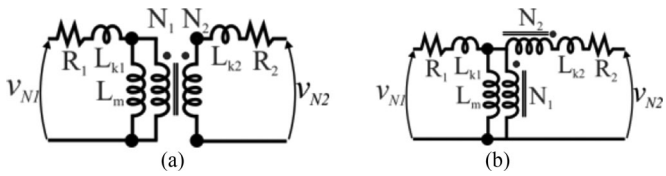

Fig. 1. Diagram of (a) transformer/coupled inductor and (b) autotransformer/tapped inductor.

Conversely, isolated single-ended topologies such as boost [13], forward, flyback, zeta, Cúk, and SEPIC, in addition to using a switch duty-cycle, can also make use of the coupled-inductor turns-ratio (N) to adjust the converter output voltage. Thus, N contributes to the voltage gain, alleviating the converter duty cycle and reducing conduction losses when compared to their nonisolated counterparts.

In practice, transformers and coupled inductors suffer from nonidealities that counterbalance their benefits. These nonidealities can be viewed in Fig. 1(a), which depicts a diagram of a transformer electrical model. In addition to the ideal transformer turns-ratio, given by (1), the leakage inductances (L_{k1}, L_{k2}) and winding resistances (R_1, R_2) play an essential role in transformer losses. The winding resistances dissipate energy due to the Joule effect and their values are proportional to the wiring length [14] and, thus, may increase when the winding number of turns increases. On the other hand, the leakage inductances trapped energy is dissipated during the switching processes. This energy is proportional to the inductance values, which are small for tightly coupled windings, i.e., when the coupling factor approaches unity. Nonetheless, the coupling factor decreases when the difference between the primary and secondary winding number of turns increases, which occurs for large values of N

$$(V_{N2}/V_{N1}) = (N_2/N_1) = N. \tag{1}$$

An alternative approach to reduce the turns-ratio value and minimize the above-mentioned effects is to adopt the

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TABLE I
TURNS-RATIO FOR THE TRANSFORMER (T) AND THE AUTOTRANSFORMER (AT)

V_{N2}/V_{N1}	2	3	4	5	6	7	8	9	10
Trafo (T)	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
Autotrafo (AT)	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0
Cu reduction (%)	50.0	33.3	25.0	20.0	16.7	14.3	12.5	11.1	10.0

autotransformer winding arrangement, which improves the voltage gain [see (2)]. The circuit diagrams are shown in Fig. 1. It can be seen from Table I that the percentage rate of copper reduction depends on the transformer turns-ratio and can reach 50% for a turns-ratio of two [15], [16]

$$(V_{N2}/V_{N1}) = (N_2/N_1) + 1 = N + 1 = N'. \qquad (2)$$

As long as galvanic isolation is often not required, another way to use the turns-ratio to adjust voltage levels between primary and secondary windings is by using coupled-inductors [18]–[21]. In such approach, the rectified secondary winding voltage contributes to boost the converter output voltage.

In order to avoid coupled-inductor leakage inductance issues and also other magnetic device loss mechanisms, voltage multiplier circuits with diode-capacitors circuits [22]–[24] as well as with voltage lift circuits [25]–[27] are also employed. The former may appear as a half-wave (or full-wave) series multiplier (Greinacher/Cockcroft–Walton) [22], [23]; a Dickson charge pump [24]; or a simple voltage-doubler [25]. On the other hand, the latter presents some few circuit variations, named self-lift [26], super-lift [27], [28], and additional series (also known as double/enhance circuit) [28].

More recently, switched inductor [29], [30], [32] switched capacitors [31], [32], and impedance-source circuits [33]–[36] have been proposed.

Alternatively to those topologies based on circuit modifications, other topologies achieve a high conversion ratio with the association of two or more dc–dc converters in cascade. This technique provides a voltage gain that is achieved by multiplying the gain of each cascaded PWM cell. Usually, the converters which make use of two cascaded cells are known as "quadratic converters" [37]–[39]. Although the voltage gain is increased, a side effect is the reduction of efficiency since it is also obtained by multiplying the efficiency of each PWM cell. In addition to cascaded cells, stacked PWM cells also have been presented in [40]–[44]. In this case, instead of processing the same power in each PWM cell, the power is shared among the staked PWM cells, which reduces the losses and improves efficiency. However, the voltage gain of the stacked converter is obtained by adding together the gain of each cell, which provides smaller values when compared to its cascade counterpart.

Since either PWM cell association (cascaded or stacked) combined to transformer/autotransformer (coupled/tapped inductor) topologies seems to be advantageous, this paper proposes a comparative evaluation of a set of high step-up dc–dc converters based on the aforementioned concepts applied to the boost and ZC PWM cells as a case study. The comparative analysis is carried out by setting a predefined voltage gain for all topologies and evaluating the following converter characteristics:

1) static voltage gain;
2) power loss distribution;
3) voltage and current stresses;
4) component stress factors (CFSs);
5) power density; and
6) efficiency.

It is important to mention that isolated topologies such as the full-bridge, half-bridge [45], and push–pull [46] are outside of the scope of this paper since they require two or more active power switches to operate properly.

This paper is organized as follows: Section II introduces a methodology to generate single-switch high-voltage step-up topologies based on the association of well-known dc–dc PWM cells. In order to understand the methodology, in Section III, a case study for boost and ZC cells is presented. In this section, four merged topologies and three already known converters are discussed. Aiming to identify advantages and limitations of the proposed high-voltage step-up topologies, the converters presented in Section III are analyzed and some of their key aspects are studied in Section IV. Section V presents the experimental evaluation of the converters. Finally, Section VI presents the conclusion from the analysis and experimental results.

TABLE II
PRIMARY CATEGORIES OF PWM CELLS AND THEIR STATIC VOLTAGE GAINS

Category	Converter	Voltage Gain	
Category S	Boost	$1/(1-D)$	(3)
(Standard PWM	Buckboost, Cuk, SEPIC, Zeta	$D/(1-D)$	(4)
cells)			
Category SI	Boost$*$	$N/(1-D)$	(5)
(Std. Isolated	Forward	ND	(6)
PWM cells)	Flyback, Cuk$*$, SEPIC$*$, Zeta$*$	$ND/(1-D)$	(7)
Category SAT	Boost$^+$	$N'(1-D)$	(8)
(Std.			
Autotransformer	Forward$^+$	$N'D$	(9)
PWM cells)	Flyback$^+$, Cuk$^+$, SEPIC$^+$, Zeta$^+$	$N'D/(1-D)$	(10)

$*$Isolated counterpart.
$^+$ Autotransformer counterpart.

II. SINGLE-SWITCH HIGH-VOLTAGE STEP-UP TOPOLOGIES

In this section, the association of PWM cells is presented in a general way. Initially, the standard dc–dc converters with voltage step-up capability are assigned as a category of converter cells, named, category S. The converters of this category (boost, buckboost, Cuk, SEPIC, and zeta) are defined as single PWM cells and they will be used in the following analyses as one of the three basic or primary categories of PWM cells. From Table II, it can be noted that the converters of each category can be grouped according to common static voltage gain in subgroups. This allows similar characteristics to be easily identified among all proposed categories. For instance, the boost PWM cell provides higher voltage gain while buckboost, Cuk, SEPIC, and zeta cells provide identical and slightly smaller static voltage gain when compared to that of boost. These PWM cells differ from each

other by their input and output current ripples, which may be larger in the absence of inductances or smaller in the presence of inductances.

On the other hand, the standard isolated dc–dc converters are assigned as category SI of PWM cells. The converters of this category (forward, isolated boost [13], flyback, isolated Cuk, isolated SEPIC, and isolated zeta) also represent one of the three primary categories. They differ from the other primary categories mainly due to the galvanic isolation provided by the transformer in their circuits. Besides isolation between primary and secondary transformer windings, their turns-ratio can also provide voltage level adjustment, which will be further used to augment the static voltage gain of the converters in the following analyses.

Finally, by replacing the above-mentioned transformer (or coupled inductor) with an autotransformer (or tapped inductor), the isolated PWM cells evolve to provide the third primary category of PWM cells. This category is named standard autotransformer converters, defined as category SAT. In spite of missing the galvanic isolation, the autotransformer winding arrangement provides an improvement in the magnetic device turns-ratio, which can be summarized as a turns ratio $N + 1$ when compared to its transformer counterpart.

The static voltage gain of each primary category is presented in Table II. It can be seen that the autotransformer converter provides an $N + 1$ instead of N turns-ratio. This slightly greater turns-ratio may reduce the converter losses, making it an advantage. In order to make the following analysis more concise, categories derived from SI and SAT will only be assigned once since they can be distinguished by replacing N with N' as suggested in (2).

After defining the three primary categories, it is easy to derive the secondary categories. Their converters are obtained by means of the association of two single PWM cells belonging to any of the primary categories (see Table II). It should be noted that according to circuit theory, the three terminal PWM cells can only be connected in two different ways, which result in the cascaded or stacked configurations. In the former configuration, the output of the first PWM cell is connected to the second PWM cell. Thus, the input terminals of the merged converter are the input terminals of the first PWM cell while the merged converter output terminals are the same as the output terminals of the second cell. In this configuration, the energy is processed twice, which greatly enlarges the static voltage gain, reducing the merged converter efficiency. In the latter configuration, the input terminals of each PWM cell are placed in a parallel-like arrangement and merged. Their output terminals, on the contrary, are stacked in a series-like arrangement. This configuration allows the sharing of the power processing, reducing the losses. Nevertheless, the staked output terminals yield only the sum of each PWM cell output voltage, which is less advantageous when compared to the cascaded configuration.

Since any combination of PWM cells belonging to the three primary categories is permitted, there will be five secondary categories corresponding to the cascaded configuration described above (see Table III) and another five secondary categories related to the stacked configuration (shown in a summarized form in Table IV). As previously defined, "S" stands for standard, "SI" for standard isolated, and "SAT" for standard with an autotransformer. Each of the PWM cell configurations yields a merged topology that can be arranged of that a single switch is employed. See [47] for a detailed discussion of the rules for achieving circuit simplification.

TABLE III
EXAMPLES OF CASCADED SECONDARY CATEGORIES OF PWM CELLS AND THEIR VOLTAGE GAINS

Category	Merged Converter	Voltage Gain	
2S-C	Quadratic Boost	$1/(1-D)^2$	(11)
	Boost (Buckboost, Cuk, SEPIC, Zeta)	$D/(1-D)^2$	(12)
SSI-C (for N)	Quadratic isolated Boost	$N/(1-D)^2$	(13)
SSAT-C (for N')	Boost-Forward	$ND/(1-D)$	(14)
	Boost-Isolated (Flyback, Cuk, SEPIC, Zeta)	$ND/(1-D)^2$	(15)
SISAT-C	Isolated Boost-Forward	$N'ND/(1-D)$	(16)
	Isolated Boost (Flyback, Cuk, SEPIC, Zeta)	$N'ND/(1-D)^2$	(17)
2SAT-C	Coupled Inductor Boost-Forward	$(N')^2 D/(1-D)$	(18)

TABLE IV
EXAMPLES OF STACKED SECONDARY CATEGORIES PWM CELLS AND THEIR VOLTAGE GAINS

Category	Merged Converter	Voltage Gain	
2S-S	Boost (Buckboost, Cuk, SEPIC, Zeta)	$(1+D)/(1-D)$	(19)
SSI-S (for N)	Boost-Isolated Boost	$(N+1)/(1-D)$	(20)
SSAT-S (for N')	Boost-Isolated (Flyback, Cuk, SEPIC, Zeta)	$(ND+1)/(1-D)$	(21)
SISAT-S	Isolated Quadratic Boost	$(N+N')/(1-D)$	(22)
	Isolated Boost (Flyback, Cuk, SEPIC, Zeta)	$(N+N'D)/(1-D)$	(23)
2SAT-S	Boost (Flyback, Cuk, SEPIC, Zeta)	$(1+D)N'/(1-D)$	(24)
	Boost-Forward	$\frac{N'(1+D(1-D))}{1-D}$	(25)
	Forward (Flyback, Cuk, SEPIC, Zeta)	$N'(1-D)/(1-D)$	(26)

This methodology of PWM cell configuration can be extended to yield the tertiary PWM cells categories. It is only necessary to associate again a single PWM cell, from any of the primary categories to a secondary PWM cell defined in Tables III and IV. Since it would take too much time and space to derive all possible tertiary categories, only two associations of PWM cells are presented in Table V in order to illustrate some of them. One is defined as category S(SSI-S)-C and the other as category S(SSAT-S)-C.

All merged PWM cells derived in Tables III–V yield a higher static voltage gain and also retain the main features of their standard PWM cells, which is crucial to carrying out the static and dynamic analyses of such dc–dc converters. Although none of the topologies are presented in this section, a case study is presented in the following section. Some of the PWM cells for

TABLE V
EXAMPLES OF TERTIARY PWM CELLS CATEGORIES AND VOLTAGE GAINS

Category	Merged Converter	Voltage Gain	
S(SSI-S)-C	Quadratic Boost-Isolated Boost	$\frac{N+1}{(1-D)^2}$	(27)
	Quadratic Boost-Isolated Converter	$\frac{ND+1}{(1-D)^2}$	(28)
S(SSAT-S)-C	Quadratic Boost Nonisolated Converter (Buckboost, Cuk, SEPIC, Zeta)	$\frac{ND+1}{(1-D)^2}$	(29)

TABLE VI
CONVERTER SPECIFICATIONS

Specification	Value	Specification	Value
Output Power, P_o	250 W	Input Voltage, V_i	30 V
Switching Frequency, fs	100 kHz	Output Voltage, V_o	240 V

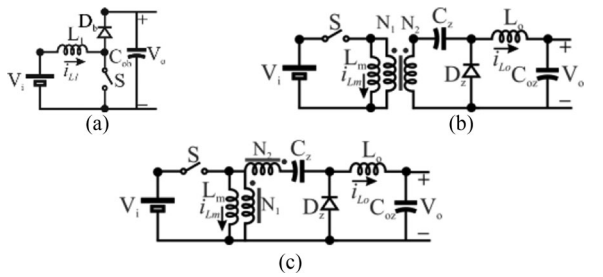

Fig. 2. Converters of the primary categories of PWM cells. (a) Boost converter (BC). (b) Isolated zeta converter (ZC) [16]. (c) Zeta with autotransformer converter (ZwAT) [16].

primary, secondary, and tertiary categories are evaluated and discussed.

III. CASE STUDY: STANDARD BOOST AND ZETA PWM CELLS

In order to discuss the features of some PWM cells and to evaluate their benefits and limitations, eight converters have been chosen. The topologies are compared according to a set of specifications presented in Table VI.

The well-known standard PWM cells, defined here as primary categories, are represented by the boost converter (BC), the isolated ZC, and the ZC with autotransformer (ZwAT) [48]. These topologies are depicted in Fig. 2(a), (b), and (c), respectively, and their voltage gains are given in Table II by expressions (3), (7), and (10), respectively. The BC is chosen as the simplest voltage step-up converter and will be the benchmark for the following analyses. The choice of ZC, on the other hand, is twofold. First, it permits an evaluation of the benefits of using a transformer as well as an autotransformer. Second, the *LC* output filter of ZC and ZwAT topologies can reduce the output voltage ripple more effectively, which may yield high power densities for these converters. Taking into account the small ripple analysis [14], all capacitors of the analyzed converters are assumed to keep their voltage at constant values during the switching period (T),

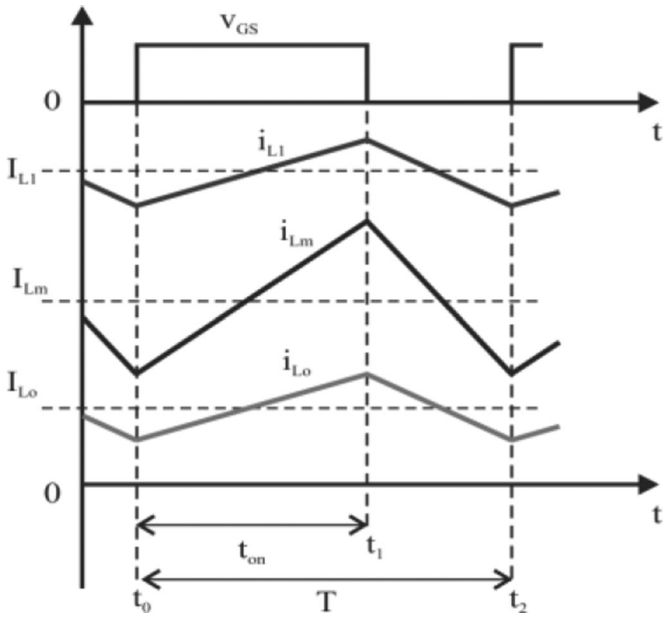

Fig. 3. Key waveforms of the converters at CCM operation.

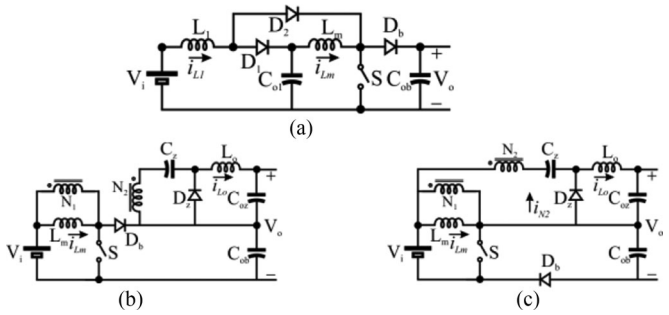

Fig. 4. Converters of the secondary categories of PWM cells (a) Cascaded boost converter or quadratic boost converter (B^2C). (b) Stacked boost–zeta converter (BZ) [17]. (c) Stacked boost–zeta with autotransformer (BZwAT) [18].

and thus, their operating modes and current stresses are only dependent on their load and inductor currents. The key inductance currents for BC (i_{L1}) and ZC (i_{Lm} and i_{Lo}) operating in continuous conduction inductor current mode (CCM) are depicted in Fig. 3.

The secondary categories are represented by the quadratic BC (B^2C), which is formed by the cascaded configuration of category 2S-C (see Table III); by the boost–zeta (BZ) converter [49], which is formed by the stacked configuration of category SSI-S (see Table IV); and by the boost–zeta converter with autotransformer (BZwAT) [50], which is formed by the stacked category SSAT-S (see Table IV). These converters are shown in Fig. 4 and their voltage gains are presented in Table III [see (11)] and Table IV [see (21)]. The cascaded association is characterized by the multiplication of the voltage gain of each cell, leading to a significant increase of the voltage conversion ratio of the merged topology. However, the full power is processed by each of the cascaded cells, reducing the converter efficiency. On the

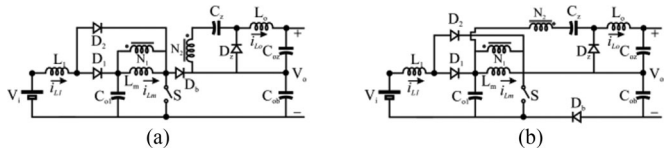

Fig. 5. Converters of the tertiary categories of PWM cells (a) Quadratic boost zeta converter (B^2Z) [11]; and (b) Quadratic boost zeta with autotransformer converter (B^2ZwAT).

other hand, the stacked association has the benefit of the power processing sharing, which minimizes the losses. Nevertheless, the achieved voltage gain is only the sum of the voltage gain of each cell. As long as these topologies are derived from the converters of primary categories, their key current waveforms still hold their characteristics and can be approximated to the waveforms shown in Fig. 3. It can be observed that i_{L1} and i_{Lm} are the currents through the inductances of B^2C while i_{Lm} and i_{Lo} are the currents through the inductances of BZ and BZwAT topologies.

Fig. 4 shows two topologies derived from the use of three PWM cells, i.e., the tertiary categories. The converters are the quadratic boost ZC (B^2Z) [51], Fig. 5(a), and the quadratic boost zeta with autotransformer (B^2ZwAT), Fig. 5(b), and their voltage gains are defined in Table V, (28) and (29), respectively. In both topologies, the cascaded and stacked associations are combined. For these converters, the key waveforms can also be approximated to those of Fig. 3, where i_{L1}, i_{Lm}, and i_{Lo} are presented in both B^2Z and B^2ZwAT.

IV. Comparative Analyses

Aiming to provide a quantitative analysis of the converters derived and discussed in the previous sections, the following six important aspects are analyzed throughout this section [52]–[59]. These aspects are evaluated taking into account that all converters operate in CCM:

1) the static voltage gain of the topologies;
2) their component count;
3) their CSF;
4) the semiconductor voltage and current stresses; and
5) the converter power density (CPD) of the converter.

A. Static Voltage Gain (M)

The static voltage gain for any PWM cell is obtained according to [47] by computing the volt-second balance of its inductances or magnetizing inductances, depending on the topology.

In the case of converters of primary categories, the voltage gain of the topology is the same as their well-known PWM cells. This way, the voltage gains for BC, ZC, and ZwAT are given by expressions (3), (7), and (10), respectively.

For the converters of secondary categories with cascaded connections, each of their PWM cell gains is multiplied together, leading to the expression (11) for the B^2C topology. Similarly, the converters of secondary categories with stacked connections have their voltage gain obtained by the sum of each PWM cell gain alone, yielding expression (21) for BZ (using N) and BZwAT (using $N = N'$).

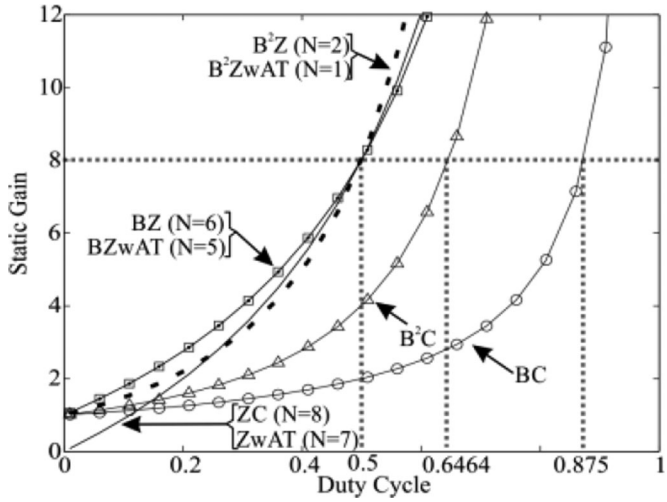

Fig. 6. Static voltage gain (M) versus of duty cycle (D) by turns ratio (N).

Converters of tertiary categories combine the multiplication and the sum of their PWM cell gains, resulting in the expressions (28) and (29) for B^2Z and B^2ZwAT, respectively. In order to evaluate the voltage gain expressions, they have been plotted in function of duty cycle in Fig. 6.

Since the turns-ratio affects the topologies in different ways, all topologies with magnetically coupled devices have their turns-ratio (N or N') calculated in order to achieve the voltage static gain eight (8) exactly at 0.5 duty cycle.

It can be seen that at a duty cycle (D) equal to 0.5, all topologies with transformer/autotransformer present twice the voltage gain of B^2C and four times that of the BC. It can be observed that for $D < 0.5$ converters, BZ and BZwAT present higher-voltage gain at the price of using a turns-ratio equal to 6 and 5, respectively. On the contrary, for $D > 0.5$ converters B^2Z and B^2ZwAT present higher voltage gain with a turns-ratio equal to 2 and 1, respectively. Finally, the converters with a turns-ratio near unity that achieved the voltage gain of eight at exactly $D = 0.5$ may present smaller copper and leakage inductance losses, which can improve their efficiency.

B. Component Stress Factor and Component Count

CSF is a parameter that measures the weighted volt-ampere stress per converter output power ratio for every single component of a converter [52], [53]. The CSF can be summed to form a total CSF for each component type. It can be used to aid the designer in identifying the limits of relative efficiency and size that can be achieved by the evaluated converters.

In the following analysis, for switches (SSCSF) and for diodes (SDCSF), a semiconductor CSF will be determined while a winding CSF will be determined for the magnetic devices (WCSF) and a capacitor CSF for all capacitors (CCSF) of each converter in the analysis. Then. for each topology, the component factors of the same type are summed, resulting in the

TABLE VII
TOTAL COMPONENT STRESS FACTORS AND COMPONENT COUNT FOR SELECTED TOPOLOGIES

Component Stress Factor (Component count)	Primary Categories			Secondary Categories			Tertiary Categories	
	BC	ZC	ZwAT	$\mathbf{B^2C}$	BZ	BZwAT	$\mathbf{B^2Z}$	$\mathbf{B^2ZwAT}$
Total S_S CSF (Switch count)	8 (1)	**2** (1)	**2** (1)	16 (1)	**2** (1)	**2** (1)	3 (1)	3 (1)
Total S_D CSF (Diode count)	8 (1)	4 (1)	4 (1)	8.49 (3)	6 (2)	6 (2)	**7** (3)	**7** (3)
Total WCSF (Winding count)	**1** (1)	4 (3)	3.75 (3)	3.83 (2)	5 (3)	4.66 (3)	6 (4)	5.5 (4)
Total CCSF (Capacitor count)	1 (1)	2 (2)	2 (2)	2 (2)	3 (3)	3 (3)	4 (4)	4 (4)
Sum of CSF (Sum of comp. counts)	18 (4)	12 (7)	11.75 (7)	30.32 (8)	16 (9)	15.66 (9)	20 (12)	19.5 (12)

following expressions:

$$\text{Total } S_S\text{CSF} = \sum_{\text{Switch}} S_S\text{CSF}_i \tag{30}$$

$$\text{Total } S_D\text{CSF} = \sum_{\text{Diodes}} S_D\text{CSF}_i \tag{31}$$

$$\text{Total WCSF} = \sum_{\text{Windings}} \text{WCSF}_i \tag{32}$$

$$\text{Total CCSF} = \sum_{\text{Capacitors}} \text{CCSF}_i. \tag{33}$$

Equations (30)–(33) are calculated taking into account the converter specifications (see Table VI) and the results are summarized in Table VII. The component count for each type of CSF is also informed aside. The results show that the CSF for switches is smaller for ZC, ZwAT, BZ, and BZwAT topologies. It points to the fact that the coupled-inductor turns-ratio helps significantly to attain voltage gain without penalizing the switch. Comparing the zeta-based converters from secondary (SSCSF $=$ 2) and tertiary (SSCSF $=$ 3) categories, it can be noticed that the cascaded PWM cell of the latter imposes more stress on the switches.

Conversely, the analysis for the diodes shows that the topologies with a large component count and smaller CSF are more advantageous, putting $\mathrm{B^2Z}$ and $\mathrm{B^2ZwAT}$ in the best position.

Analogously, with respect to magnetic devices, the WCSF is best for the single inductor BC. This reveals that the turns-ratio of coupled inductors always impose more stress on winding with a great number of turns, which becomes a disadvantage for zeta-based converters. On the other hand, the autotransformer arrangement provides a reduction of turns-ratio and decreases WCSF of all SAT category converters when compared to their SI category counterparts.

For the capacitors, it is shown that the CCSF is the same for all evaluated converters.

The sum of each CSF is also computed, showing that $\mathrm{B^2ZwAT}$ and $\mathrm{B^2Z}$ are the first and second smallest values, respectively.

C. Absolute Maximum Semiconductor Voltage Ratings

The maximum tolerable limits of the applied voltage are defined as the maximum ratings for that device. Together with the maximum allowable current and power dissipation, the absolute maximum ratings are important and the device must not experience a condition under which any one of the limits abovementioned is exceeded.

TABLE VIII
ABSOLUTE MAXIMUM VOLTAGE RATINGS FOR SEMICONDUCTORS

	Prim. Categories		Sec. Categories		Ter. Categories
	BC	ZC/ ZwAT	$\mathrm{B^2C}$	BZ/ BZwAT	$\mathrm{B^2Z}$/ $\mathrm{B^2ZwAT}$
S	$\frac{1}{1-D_M}V_i$	$\frac{1}{1-D_M}V_i$	$\frac{1}{(1-D_M)^2}V_i$	$\frac{1}{1-D_M}V_i$	$\frac{1}{(1-D_M)^2}V_i$
D_b		–			
D_z	–	$\frac{N}{1-D_M}V_i$	–	$\frac{N}{1-D_M}V_i$	$\frac{N}{(1-D_M)^2}V_i$
D_1	–	–	–	–	$\frac{1}{(1-D_M)^2}V_i$
D_2	–	–	–	–	

D_M is the maximum operating duty-cycle.
Turns-ratio is N for BZ, $\mathrm{B^2Z}$; and N' for BZwAT, $\mathrm{B^2ZwAT}$.

The drain–source voltage limit ($\mathrm{BV_{DSS}}$) for a MOSFET device is the largest voltage it can hold and for $\mathrm{BV_{DSS}}$ greater than a few hundred volts, the drain drift region resistance (R_d) dominates the ON-state resistance (R_{DSon}) of the device. Under such conditions, R_d [57] can be roughly estimated as $R_d \approx k \cdot \mathrm{BV_{DSS}}^{2.5-2.7}$.

In other words, the MOSFET ON-state resistance increases with $\mathrm{BV_{DSS}}$, and high breakdown voltage devices will lead to high conduction losses.

The voltage stresses on the semiconductors are obtained by analyzing the OFF-state for switches and diodes of each topology. The maximum direct voltage across the switch is considered to be the switch absolute maximum allowable voltage. On the other hand, the maximum reverse voltage across each diode is defined as its absolute maximum voltage rating. The absolute voltage ratings for each semiconductor device of all analyzed converters are presented in Table VIII. The expressions are defined as a function of the input voltage (V_{in}) and the maximum duty cycle (D_M) that is designed for the converter at its operating point.

It can be seen that the switch and boost diode (D_b) voltage stresses always depend on the boost or quadratic boost cell gain, regardless of the transformer turns-ratio. Conversely, the turns-ratio (N or N') is proportionally related only to the zeta diode D_z.

D. Converter Power Density (CPD)

An important parameter characterizing the compactness of power converters is the ratio of converter output power and

TABLE IX
DESIGN CONSIDERATIONS OF CONVERTERS

	Primary Categories			Secondary Categories			Tertiary Categories	
	BC	ZC	ZwAT	B²C	BZ	BZwAT	B²Z	B²ZwAT
D (N)	0.875 (-)	0.5 (8)	0.5 (7)	0.6464 (-)	0.5 (6)	0.5 (5)	0.5 (2)	0.5 (1)
Inductors (mag. core) L^+, R_{DC^+}	L_m: 93.75 µH (77192*) R_{DC}: 89 mΩ	L_m: 94 µH (77083*) R_{DC}: 163 mΩ L_k: 2.6 µH L_o: 13.86 mH (77192*) R_{DC}: 1.42 Ω+	L_m: 81 µH (77083*) R_{DC}: 124 mΩ L_k: 2.2 µH L_o: 12 mH (77192*) R_{DC}: 1.31 Ω+	L_1: 93.75 µH (77083*) R_{DC}: 36mΩ L_m: 150 µH (77076*) R_{DC}: 55mΩ	L_m: 94.2 µH (77083*) L_k: 1.6 µH R_{DC}: 112mΩ L_o: 10.1 mH (77439*) R_{DC}: 1.42 Ω	L_m: 76 µH (77083*) L_k: 1.5 µH R_{DC}: 101 m Ω L_o: 8.2 mH (77439*) R_{DC}: 1.31 Ω	L_1: 131 µH (77071*) R_{DC}: 610 mΩ L_m: 192 µH (770839*) R_{DC}: 50 mΩ L_k: 1.4 µH L_o: 7.5 mH (77071*) R_{DC}:0.78Ω	L_1: 130 µH (77071*) R_{DC}: 534 mΩ L_m: 96 µH (770839*) R_{DC}: 24 mΩ L_k: 1.3 µH L_o: 3.2 mH (77071*) R_{DC}: 0.66 Ω
Capacitors	C_{ob}:9 µF (0.12Ω+)	C_z:270nF (0.13Ω+) C_{oz}:12nF (0.12Ω+)		C_{o1}: 8 µF (0.32Ω+) C_{ob}: 4 µF (0.12Ω+)	C_z: 1 µF (0.15Ω+) C_{oz} :47 nF (0.23Ω+) C_{ob} : 4 µF (0.16Ω+)		C_z: 3.3 uF (0.36Ω+) C_{oz}: 180 nF (0.19Ω+) C_{o1}:16 µF (0.32Ω+) C_{ob}: 9 µF (0.15Ω+)	
Switch BV_{DSS} / I_{DM} ($R_{DS(on)}$, C_{oss}) (t_{on}, t_{off}) $R_{\theta(jc)}$	IRFP450N 500 V/ 14 A (0.99Ω, 2410 pF) (83 ns, 91 ns) 0.64 °C/W	IRFP250N 200 V/ 30 A (0.64 Ω, 315 pF) (58 ns, 84 ns) 0.7 °C/W		IRFP450N 500 V/ 14 A (0.99Ω, 2410 pF) (83 ns, 91 ns) 0.64 °C/W	IRFP150N 100 V/ 42 A (0.17 Ω, 450 pF) (66 ns, 96 ns) 0.95 °C/W		IRFP250N 200 V/ 30 A (0.64 Ω, 315 pF) (58 ns, 84 ns) 0.7 °C/W	
Diodes V_{RRM} /I_F (r_k) $R_{\theta(jc)}$	D_b STPSC4H065 650 V/4A (0.61Ω) 1.8 °C/W	D_z: STPSC4H065 650 V/ 4 A (0.61Ω) 1.8 °C/W		D_1 and D_2 MBR20200CT 200 V/20A (0.22Ω) 2.0 °C/W D_b STPSC4H065 650 V/4 A (0.61Ω) 1.8 °C/W	D_b: MBR20200CT 200 V/20A (0.22Ω) 2.0 °C/W D_z: STPSC4H065 650 V/4 A (0.61Ω) 1.8 °C/W		D_b, D_1 and D_2: MBR20200CT 200 V/20A (0.22Ω) 2.0 °C/W D_z: STPSC4H065 650 V/4 A (0.61Ω) 1.8 °C/W	
Estimated Junction Tempeture	110 °C	110 °C	110 °C	110 °C	110 °C	110 °C	110 °C	110 °C
Heatsink ($R_{\theta(SA)}$)	HS 7624 (2.1 °C/W)	HS 4425 (11.13 °C/W)		HS 7624 (4.02 °C/W)	HS 4425 (19.3 °C/W)		HS 4425 (10.75 °C/W)	
Fan	CR0412HB-C50							

* Magnetic core material from Magnetics® [58]. All capacitors are film material. Heat sink material from HS Heat sink® [59]. Fan CR0412HB-C50 [60].
+ Measured in laboratory.

converter volume. The CPD is calculated for all compared topologies and the results are discussed. The CPD depends on converter power losses and thermal management of the components, i.e., its calculation is necessary prior to designing the prototypes, to define the technology to be used for each of the converter components and the thermal management system.

Initially, the converter design assumes that all topologies will operate under the specifications presented in Table VI. Hence, the converters active and passive components are designed according to ordinary switching power supply design methodologies, such as those described in power electronics text books (for instance [14]). Taking into account that the topologies operate in CCM and applying the above-mentioned reference, the values for all components of each converter are summarized in Table IX.

To obtain the electric current and voltage variables from the converters, digital simulation provided by PSIM simulation software was used.

In order to easily compute the estimated power losses, typical switching waveforms are modeled using piecewise linear approximations. This way, turn-ON and turn-OFF switching losses can be obtained by applying the simple integral equation of device voltage and current variables during the switching intervals, as can be seen in expression (34), where t_{on} and $t_{\rm off}$ have been approximated by the rise and fall times provided in the device manufacture datasheet (see Table IX), respectively

$$P_{\rm Sw} = \frac{1}{2} V_s I_s f_s \left(t_{\rm off} + t_{\rm on}\right). \tag{34}$$

Semiconductor conduction losses can be separated into switch ON-state losses (35) and diode conduction losses (37)

$$P_{S\rm con} = {I_{S\_\rm rms}}^2 R_{\rm DS(on)} \tag{35}$$

where $I\_S\rm rms$ is the switch rms current and $R_{\rm DS(on)}$ is the MOSFET ON-state resistance obtained from device static characteristics provided by manufacture datasheet information

$$P_D = \sum_{k=1}^{K} {I_{D\rm rms(k)}}^2 r_{D(k)} \tag{36}$$

where $I_{D\rm rms}$ is the rms current and r_D is the conduction resistance of the kth converter diode. Resistance r_D is calculated from diode static characteristics given by the manufacture datasheet.

As long as the copper wire diameters obey the limits imposed by the skin effect, magnetic device losses for inductors and coupled inductors can be gathered in copper and core losses, as suggested by

$$P_L = \sum_{j=1}^{J} r_{L(j)} {I_{L\rm rms(j)}}^2 + \sum_{h}^{H} \left(a {B_{\rm pk(h)}}^b {f_s}^c\right) A_{e(h)} l_{e(h)} \tag{37}$$

where $I_{L\rm rms}$ is the rms current of the jth magnetic device winding; $B_{\rm pk}$ is the ac magnetic flux density for the hth magnetic device core; l_e is the core medium path length MPL, and A_e is the transversal core area, both given in the manufacture core information [58].

Finally, capacitor losses can be regarded as the power dissipated due to their equivalent series resistance (ESR). These

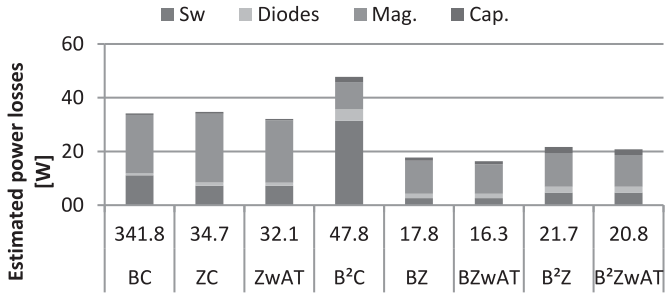

Fig. 7. Estimated losses (in Watts) for switch (Sw); diodes (Diodes); magnetic devices (Mag.); and capacitors (Cap.).

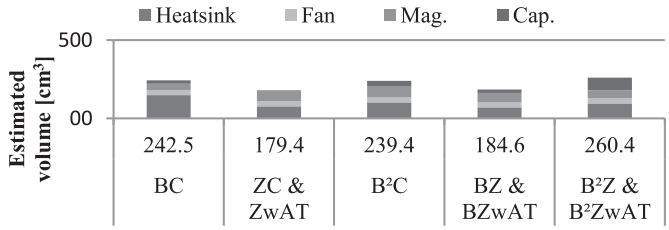

Fig. 8. Estimated volume (in cm^3) for heatsink (Heatsink); fans (Fan); magnetic devices (Mag.); and capacitors (Cap.).

losses are summarized as

$$P_C = \sum_{g=1}^{G} {I_{C\mathrm{rms}(g)}}^2 \mathrm{ESR}_{(g)} \tag{38}$$

where $I_{C\mathrm{rms}}$ is the rms current and ESR the measured resistance of the gth capacitor.

The total estimated losses and their distribution, for all evaluated converters, are shown in Fig. 7. The largest losses are presented by the BC that reached 340 W. This is a result of the higher duty cycle that imposes a great current stress on the switch (111 W of losses) and inductor (218 W of losses). The second largest loss is the 48 W of the B^2C. Compared to the BC, the duty cycle is reduced and the inductors are split, which helps to alleviate the losses. Nevertheless, the MOSFET switch alone contributes to 31 W of losses. For the other topologies, the losses are smaller since all operate at 0.5 duty cycle. The disadvantage of B^2Z and B^2ZwAT relays on the cascaded configuration is that power is processing twice, compared to the BZ and BZwAT topologies, which provide the sharing of power processing. Additionally, it can be seen that the topologies with autotransformers can slightly reduce the magnetic losses yielding the lowest loss of 16 W, achieved by the BZwAT converter.

All dissipated power must be removed to limit temperature rise within the devices since the reliability and lifetime of the converter depend on their operating temperatures. In order to keep the semiconductor operating temperatures well below their maximum allowed values, all semiconductors of a converter are mounted in a heat sink system. This system consists of an extruded aluminum heat sink with forced air flow provided by a fan (with 4 m/s) attached to the heat sink. The thermal management of the semiconductors can be accomplished by calculating the required heat sink volume to achieve the thermal resistance $R_{\theta(\mathrm{SA})}$ to keep the junction temperature at least 50 °C below its absolute maximum value, considering a 25 °C room temperature, as described in [61]. It is considered that the one-dimensional thermal radiation model at thermal steady-state conditions provides a good estimation.

On the other hand, power dissipated in the magnetic devices can count only on the surface area of the magnetic core and winding. This way, the magnetic device design procedure will ensure that the maximum temperature for the magnetic material is not reached. Similarly, the maximum allowable temperature rise of the capacitors is guaranteed by their electrothermal design. The converter estimated volumes are shown in Fig. 8. It can be seen that in spite of a lower component count, the BC topology presents one of the largest volumes (242 cm^3) due to the required prominent heat sink. The B^2C presents a similar volume (239 cm^3) with a smaller heat sink but with the largest magnetic space. The boost quadratic-based tertiary category converters present the largest volumes (260 cm^3). The smaller volume of 179 cm^3 is reached for the ZC and ZCwAT topologies due to the small heat sink dimensions. BZ and BZwAT provide a similar volume (184 cm^3).

TABLE X
CONVERTER POWER DENSITY AND RELATIVE COST

	Pri. Categories			Sec. Categories			Ter. Categories	
	BC	ZC	ZwAT	B^2C	BZ	BZwAT	B^2Z	B^2ZwAT
CPD*	0.21	0.59	0.61	0.45	0.63	0.64	0.43	0.44
RC+	100	130	130	170	150	150	230	230

* [W/cm^3]>, and + [%].

Finally, the CPD, given by (39), is defined according to [55], as twice the ratio of output power and the sum of the partial volumes shown in Fig. 8. This factor of two compensates for the volumes not taken into account, such as measurement and control circuitry plus the required area to mount all different component shapes in printed circuit board (PCB)

$$\mathrm{CPD} = 2 \times P_o \Big/ \sum_{l} \mathrm{Vol}_{(l)}. \tag{39}$$

The CPD for the evaluated topologies is shown in Table X. The highest CPD is achieved by the BZwAT with 0.64 W/cm^3. The BZ and ZwAT achieved 0.63 and 0.61 W/cm^3, respectively. The results can be considered adequate since no optimization procedure was used.

E. Converter Relative Cost

The relative cost (RC) comparison of evaluated converters is tabulated in Table X. Since the absolute costs of the components are affected by factors such as manufacturing company nominal productions, location of the manufacturing site, availability of raw material suppliers, and its transportation costs, as well as market price fluctuations and uncertainties, each component cost was evaluated comparatively to the cost of the same type of component used in the BC. This way, the actual price of the

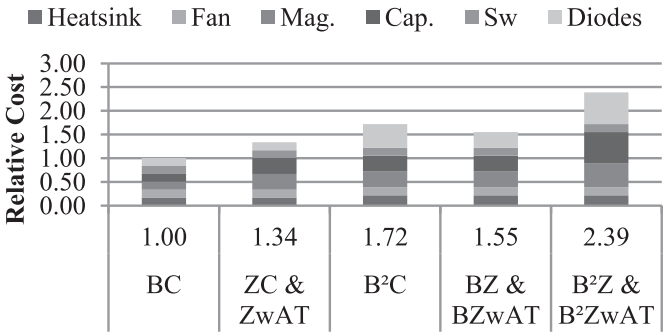

Fig. 9. Relative cost for heat sink (Heat sink); fan (Fan); magnetic devices (Magnetics); capacitors (Capacitors); switch (Others); and diodes (Diodes).

BC in certain locations of the globe can be computed and thus the RC for each topology can be used to find its actual price.

It can be observed in Table X that the number of components has a major influence since the prices increase from primary to tertiary category converters, making the B^2Z and B^2ZwAT more than twice the BC topology. It can also be seen from the secondary category converters that it is more cost worthy to use stacked topologies than cascaded ones. The disaggregated relative prices are plotted in Fig. 9, showing that the passive component costs (magnetic devices and capacitors) are the most prominent.

V. Experimental Results

In order to verify some of the main characteristics discussed in the previous theoretical analyses, eight 250 W step-up prototypes have been built. The prototype specifications are summarized in Tables VII and IX. The experimental set-up employed a dc voltage source to establish the input voltage and a controlled electronic load to set the exact constant load power value for each evaluation. The prototypes operate in open loop control at the steady-state defined by the duty-cycle presented in Table IX. The control algorithm had been developed with a TMS320F28335 Digital Signal Processor. The waveforms were obtained from a Tektronix Encore MD03000 oscilloscope and the efficiencies were acquired from a Yokogawa WT1800 power meter.

Fig. 10 shows the drain–source voltage across the MOSFETs for each prototype. It can be observed that BC [see Fig. 10(a)] and B^2C [see Fig. 10(d)] switches must withstand the entire output voltage (240 V). In addition, the duty cycles are higher among the other prototypes. On the other hand, ZC [see Fig. 10(b)] and ZwAT [see Fig. 10(c)] prototypes present the smallest voltage stresses across the switches (60 V). Furthermore, the switched duty cycles are kept at 50%. Nevertheless, a severe voltage ringing can be observed, which imposes additional stresses and losses due to the energy trapped in the leakage inductance of their coupled inductors. In contrast, voltage stress across the switches of B^2Z [see Fig. 10(g)] and B^2ZwAT [see Fig. 10(h)] are reduced by fifty percent (120 V). Meanwhile, voltage stress on BZ [see Fig. 10(e)] and BZwAT [see Fig. 10(f)] switches is reduced by seventy five percent (60 V). The boost diode of these

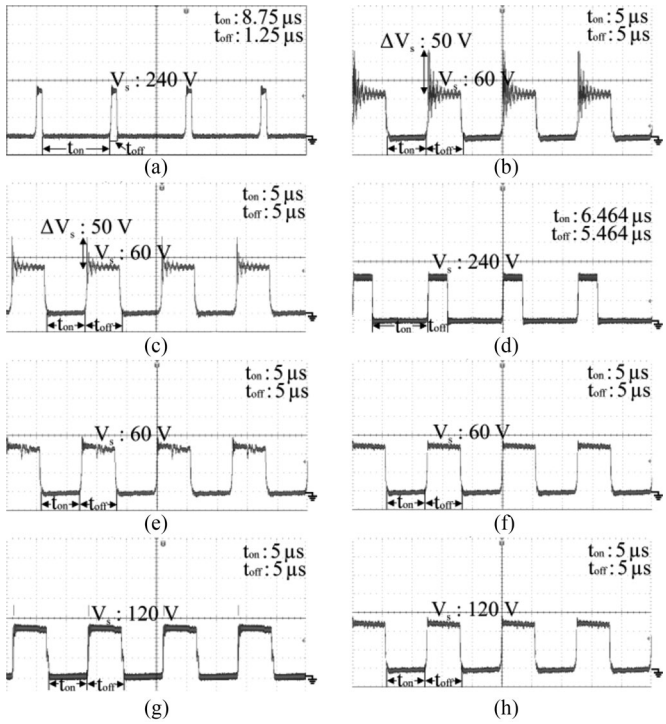

Fig. 10. Experimental voltage switch stress (V_s) waveforms (all $4\,\mu s/div$). (a) BC. (b) ZC. (c) ZwAT. (d) B^2C. (e) BZ. (f) BZwAT. (g) B^2Z. (h) B^2ZwAT.

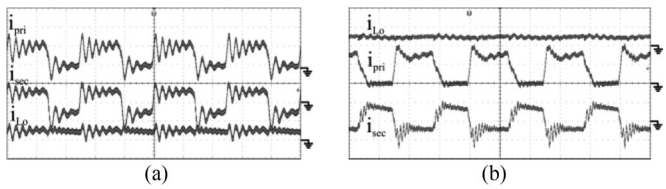

Fig. 11. Experimental currents through the inductances waveforms (all $4\,\mu s/div$): (a) ZC and (b) BZ.

converters provides a natural clamping to the coupled inductor leakage energy that is recycled to the output.

Aiming to show the effect of the leakage inductance on the evaluate topologies, Fig. 11 shows the waveforms of the current through the inductances for ZC and BZ. As can be seen in Fig. 11(a), there is a ringing due to the resonance produced mainly by the current through the coupled-inductor leakage inductance and the voltage across the MOSFET output capacitance. To reduce such ringing, it is necessary to include a snubber or clamping circuit across the MOSFET.

In contrast, Fig. 11(b) shows the correspondent waveforms for the BZ converter. A reduction of the ringing due to the natural voltage clamping provided by the boost diode and the smaller leakage inductance obtained by the reduction of the coupled-inductor turns-ratio value can be seen. It is worth to mention that ZwAT presented similar behavior as the ZC converter; meanwhile, B^2Z and B^2ZwAT presented similar waveforms as the BZ converter.

The efficiency of all prototypes was evaluated experimentally at the nominal load conditions (250 W) and compared to the estimated efficiency provided by the loss models derived in

TABLE XI
CONVERTERS EFFICIENCY

	Pri. Categories			Sec. Categories			Ter. Categories	
	BC	ZC	ZwAT	B^2C	BZ	BZwAT	B^2Z	B^2ZwAT
E∗	42.2	87.8	88.6	84.0	93.4	93.9	92.0	92.3
M^+	39.8	84.2	87.1	82.3	92.5	93.2	91.0	92.0

E∗—Estimated [%]; M^+ —Measured [%].

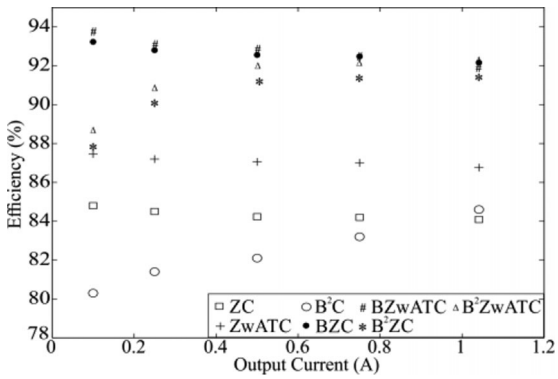

Fig. 12. Experimental efficiency curves against output current (load current).

the previous sections; the results are summarized in Table XI. It can be seen that BZ and BZwAT converters presented the highest efficiency, achieving 92% and 93%, respectively. B^2Z and B^2ZwAT prototypes reached 91%. Except for the BC, the other prototypes presented efficiency between 82% and 87%, which may be considered inadequate, since their application would require further optimization. As expected, the BC converter prototype demonstrates a very poor efficiency, of just 39%, which confirmed that this converter cannot be used for high-voltage step-up applications.

Additionally, experimental efficiency curves were obtained by varying the output current as shown in Fig. 12. It can be seen that efficiency increases with the load power for B^2C and it is quite flat for ZC and ZwAT prototypes, which indicate that coupled inductor-based converters operate more efficiently at low load conditions and conversely, B^2Cs are more efficient at high load conditions. These features explain the behavior of B^2Z and B^2ZwAT, whose efficiency is higher at full load and degrades for low load power values. On the other hand, BZ and BZwAT provide higher efficiency over the entire load range, attaining efficiencies higher than 92% for all evaluated conditions. The highest efficiency value achieved in the tests is 93.7% achieved by BZwAT.

VI. CONCLUSION

This paper presented a comparative evaluation of high step-up converters, whose topologies were obtained from the association of standard dc–dc PWM cells. A case study was carried out for eight topologies based on boost and zeta PWM cells. Features for static voltage gain, component current and voltage stresses, power losses, power density, and efficiency were addressed regarding each converter operating under the same specifications. Results demonstrated that incorporating the autotransformer concept to a stacked association of a boost and a zeta PWM cell provided a merged topology (BZwAT) with higher efficiency and power density with 50% when compared to the BC. Nevertheless, by replacing the boost cell with a quadratic boost cell (B2ZwAT), the voltage gain was much enhanced. For the input and output voltage specifications of the case study, the B2ZwAT allowed an expressive reduction of the coupled inductor turns-ratio (5 times) and the overall CSF ($\approx$6.3%). This indicated that it would be more advantageous to employ the B^2ZwAT for even higher voltage gain applications.

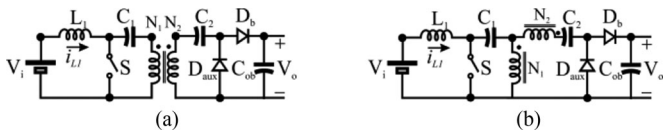

Fig. 13. Converters of the primary categories of PWM cells. (a) IBC [13]; and (b) BwATC.

APPENDIX I
CASE STUDY: STANDARD BOOST AND ISOLATED BOOST PWM CELLS

In Section II, the association of PWM cells was presented. In that section, the standard dc–dc, standard isolated dc–dc, and standard autotransformer converters had been defined. In addition, the association of two and three single PWM cells belonging to any of the primary categories had been discussed. The combination of two and three of them may generate several converters, some of them already known circuits and other new topologies. Aiming to discuss and evaluate their benefits and limitations, eight circuits based on the boost and zeta standard converters have been chosen.

In this appendix, six circuits based on the standard BC and the standard isolated BC (IBC) are presented and discussed briefly. Different from other standard isolated topologies, the IBC can provided voltage step-up even with unitary transformer turns-ratio, which ensure larger voltage gain. Nevertheless, likewise the standard boost, it presents a discontinuous output current, which may prevent its employment for some applications.

A. Static Voltage Gain (M)

The following analysis takes into account the BC [see Fig. 2(a)], the IBC [see Fig. 13(a)], and the BC with autotransformer [BwATC, Fig. 13(b)], as the three representatives of the primary categories. The voltage gain for each of these topologies is shown in Table II by expressions (3), (5), and (8).

The merged topologies of the secondary categories are represented by the cascaded BC with isolated BC [IB^2C, Fig. 14(a)] and by stacked BC with isolated BC [BIBC, Fig. 14(b)]. Their voltage gains are defined by expression (13) in Table III and expression (20) of Table IV, respectively.

The combined topology of the tertiary categories is the cascaded BC with stacked isolated BC (B^2IBC), shown in Fig. 15. Its voltage gain is defined by expression (27) of Table V.

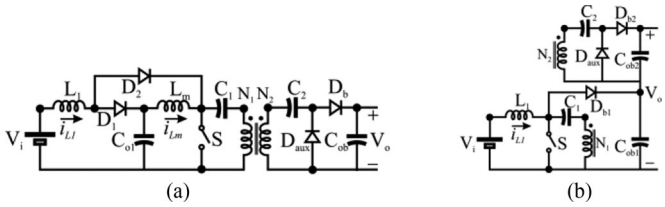

Fig. 14. Converters of the secondary categories of PWM cells (a) Cascaded BC with IBC (IB^2C); and (b) Stacked BC-IBC converter (BIBC).

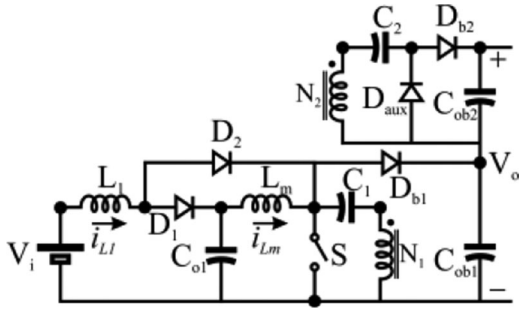

Fig. 15. Converters of the tertiary categories of PWM cells cascaded BC with stacked IBC (B^2IBC).

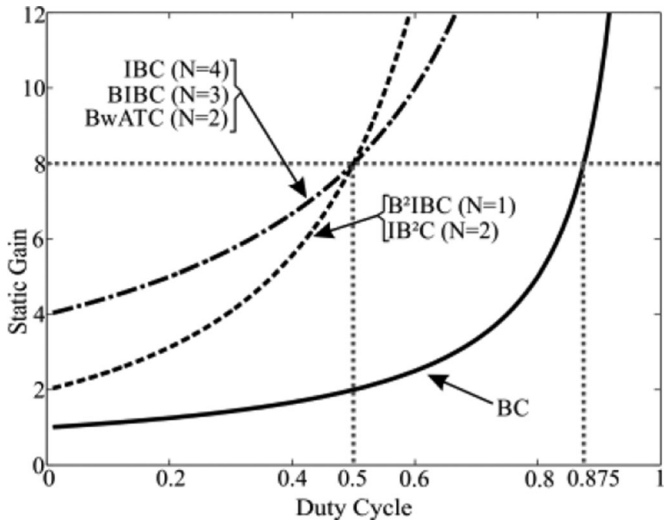

Fig. 16. Static voltage gain (M) versus duty cycle (D) by turns ratio (N).

In order to evaluate the voltage gain expressions of the converters, they have been plotted in function of duty cycle in Fig. 16. As long as the combination of duty-cycle and turns-ratio affects the topologies in different ways, the turns-ratio has been calculated in order to the voltage gain to reach eight (8) exactly at a duty cycle of 0.5.

From Fig. 16, it can be noted that IBC, BBIBC, and BwATC present voltage gains always higher than four (4), with turns-ratio of 4, 3, and 2, respectively. On the other hand, IB^2C and B^2IBC present voltage gains always higher than four (2), with turns-ratio of 2 and 1, respectively. The leakage inductance increases proportionally with the turns-ratio value; thus, smaller turns-ratio will lead to less trapped energy in the leakage ($0.5L_kI_{pk}^2$) and lesser will be the losses. In general, BwATC is advantageous at low duty cycles and B^2BIC at higher duty cycle values.

TABLE XII
ABSOLUTE MAXIMUM VOLTAGE RATINGS FOR SEMICONDUCTORS

	Prim. Categories		Sec. Categories		Ter. Categories
	BC	IBC/BwATC	IB^2C	BIBC	B^2IBC
S	$\frac{1}{1-D_M}V_i$	$\frac{N}{1-D_M}V_i$	$\frac{N}{(1-D_M)^2}V_i$	$\frac{N}{1-D_M}V_i$	$\frac{N}{(1-D_M)^2}V_i$
D_b					
D_{aux}	–				
D_1	–	–	$\frac{1}{1-D_M}V_i$	–	$\frac{1}{(1-D_M)^2}V_i$
D_2	–	–		–	

D_M is the maximum operating duty-cycle.

B. Absolute Maximum Semiconductor Voltage Ratings

The maximum tolerable limits of the applied voltage are defined as the maximum ratings for that device, presented in Table XII. As can be seen in Table XII, aside BC, all other converters, the maximum voltage stress across the switch S and output diode Db depend on the duty-cycle and the turns-ratio. This implies a higher stress of these components. In addition, comparing Table XII with Table VIII, it is evident that this set of converters presents higher absolute maximum voltage ratings.

It can be concluded in this brief analysis that the replacement of the ZCs by its isolated boost counterparts provide higher voltage gain, which may allow to reduce the converters turns-ratio. Nevertheless, the voltage stress on semiconductors is higher, requiring high-voltage breakdown semiconductors. This way, the leakage inductance may be reduced at the expense of high-voltage capability semiconductors. More analyses concerning efficiency, power density, and RC have not been carried out due to the paper size restrictions.

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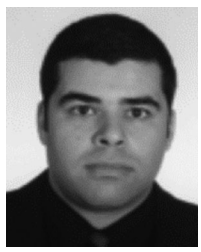

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