

Series-Connected Partial-Power Converters Applied to PV Systems: A Design Approach Based on Step-Up/Down Voltage Regulation Range

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Abstract—This paper proposes a novel approach to reduce the power processed by series-connected partial-power converters (S-PPC) applied to string/multistring level maximum power point tracking photovoltaic systems. A design procedure based on the definition of the voltage regulation range is presented. It introduces an additional degree of freedom that allows a proper design of the converter in order to reduce not only the active power but also the nonactive power, reducing losses and increasing power density. By means of the proposed approach, it is also demonstrated that by replacing the conventional step-up partial-power converter by a step-up/down partial-power converter, the active and nonactive power can be further reduced, allowing to better explore the benefits of the partial-power concept. In order to validate the proposed approach, two 750-W prototypes of full-bridge S-PPC and full-bridge/push-pull S-PPC were implemented and experimentally evaluated. The step-up/down prototype presented a reduction of 46.9% in nonactive power and 23.4% of its volume, resulting in a higher efficiency and power density in comparison to the voltage step-up prototype counterpart.

Index Terms—DC-DC power conversion, design methodology, photovoltaic (PV) power systems, series-connected partial-power converters (S-PPC), string-level MPPT.

I. INTRODUCTION

THE increasing demand for electricity and environmental concerns related to fossil fuel based sources is encouraging the use of renewable sources, among them photovoltaic (PV) systems. In order to make these systems competitive compared to ordinary hydro or thermal power plants, several researches are being carried out with the objective of not only improving

Manuscript received April 13, 2017; revised August 21, 2017; accepted October 10, 2017. Date of publication October 22, 2017; date of current version June 22, 2018. This work was supported by the National Council for Scientific and Technological Development (CNPq) and Coordination of Improvement of Higher Education Personnel (CAPES). The work of H. L. Hey was supported by research grant CNPq—Brazil under Grant 309214/2013-0, Grant 462247/2014-7, and Grant 465640/2014-1. Recommended for publication by Associate Editor V. Agarwal. (Corresponding author: Jonatan Rafael Rakoski Zientarski.)

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Digital Object Identifier 10.1109/TPEL.2017.2765928

the performance of PV modules but also of increasing the efficiency of the electronic converters employed as their interface to the grid. Among different approaches, partial-power converters (PPC) are presented as strong candidates to improve the overall efficiency and power density of the dc-dc stage applied to voltage regulation and maximum power point tracking (MPPT) of PV systems [1]–[8].

The main goal of PPC is to process just a small amount of the total power, allowing the largest fraction of power to be directly delivered to the load without being processed by the converter circuit [4], [5]. With a small portion of power processing, the power converter has a small active power rating and the overall efficiency can be increased. The PPC concept can be implemented in two ways: by using parallel-connected partial-power converters (P-PPC) or using series-connected partial-power converters (S-PPC). The P-PPC, also called differential power processing (DPP), provides current regulation by including a parallel current path to the string current, allowing individual MPPT in strings of PV modules under partial shading conditions [9]–[11]. On the other hand, S-PPC can provide voltage regulation for string or multistring inverter PV systems connected to a common dc bus by means of a series-connected dc-dc converter.

Several studies have been carried out employing S-PPC in string/multistring inverter PV systems exhibiting better efficiency and reduced power rating compared to standard full-power processing topologies [1]–[3], [6], [7], [12], [13]. However, not all converter topologies connected in the S-PPC configuration can really process a smaller amount of power compared to a full-power counterpart. In some cases, the S-PPC configuration only reduces the active power but exhibits an increase in nonactive and total power processed, providing no loss reduction and efficiency improvement [14], [15]. It is a consequence of some important losses mechanisms to be dependent on both, active and nonactive power [16]. Even topologies that can perform partial-power processing may process more or less power depending on several design parameters, such as voltage regulation range, duty cycle, and transformer turns ratio. It means that only a well-designed S-PPC can improve energy harvesting of PV systems.

In a conventional design approach, which employs full-power processing topologies, the voltage regulation range (Δv) is not a critical design parameter since it does not define the active

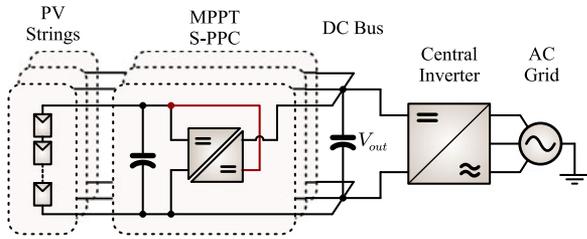


Fig. 1. String-level MPPT architecture employing S-PPC dc-dc converters.

power of the converter. In S-PPC topologies, however, the value of Δv is highly relevant design parameter as it does define both active and nonactive power processing, affecting the size of components and the overall system performance. The previously published studies on S-PPC do not consider the proper Δv for voltage step-up or step-up/down S-PPC topologies. Therefore, in this paper, the authors propose an analysis of the proper voltage range of operation of S-PPCs based on statistical models of climate conditions applied to PV modules. This paper also presents a comparison between a voltage step-up and a voltage step-up/down S-PPC topologies in order to demonstrate the benefits and limitations of the employment of step-up/down S-PPC topologies, where a full-bridge/push-pull (FB/PP) S-PPC topology, which can operate as voltage step-up/down, is compared to a dc-dc full-bridge S-PPC topology, which can only operate as voltage step-up.

These two topologies are also analyzed in terms of nonactive power and in terms of their component stress factor (CSF). The comparison shows that for the same input voltage range and power levels, the FB/PP S-PPC processes less energy and has fewer component stresses than a full-bridge S-PPC, having better power density and efficiency.

II. S-PPC APPLIED TO PV SYSTEMS

Because of its partial-power processing characteristic, S-PPCs are suitable for PV systems in string/multistring inverter MPPT architecture, as shown in Fig. 1 [1]–[3]. In this architecture, each string or arrangement has its own MPPT regulator, and the dc bus voltage is controlled by the central inverter [17]. Since the operation of a PV module has a small range of voltage variation, it allows the S-PPCs to be designed with low active power rating, processing only the amount of energy required to regulate the string's voltage and current levels.

The S-PPC configuration can be seen as a lossless dummy converter [18], which can be connected in two ways: with a series connection to the dc-dc converter output terminals (type I) or with its input terminals (type II), as shown in Fig. 2(a) and (b), respectively. In most cases, the converter topology must be isolated to not cause a short between input and output potentials.

A. Active Power and Efficiency

In comparison to type-II, type-I presents better performance in terms of efficiency and stress over its components [18]. In the type-I configuration, the value of V_C is the difference be-

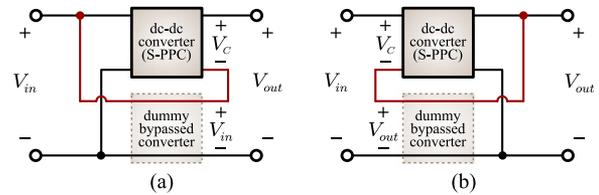
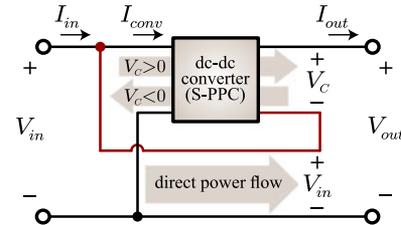


Fig. 2. S-PPC connection schematics [18]. (a) Type-I. (b) Type-II.


 Fig. 3. S-PPC type I power flow considering $V_C > 0$ (voltage step-up) and $V_C < 0$ (voltage step-down).

tween the dc bus voltage (here called output voltage, V_{out}) and the input voltage (V_{in}). The lower this difference, the lower the active power processed by the S-PPC ($P_{C_{out}}$) compared to the total output active power (P_{out}) as demonstrated by (1) [19]. When the voltage gain ($M = V_{out}/V_{in}$) gets closer to one, the active power on the converter approaches zero

$$\frac{P_{C_{out}}}{P_{out}} = \frac{V_C I_{out}}{V_{out} I_{out}} = \frac{V_{out} - V_{in}}{V_{out}} = 1 - \frac{V_{in}}{V_{out}}. \quad (1)$$

Since the active power in the S-PPC is only a portion of P_{out} , the overall efficiency (η_{global}) is greater than that measured on the S-PPC's terminals and can be calculated by (2) [4]

$$\eta_{global} = \frac{P_{out}}{P_{in}} = 1 - \frac{P_{C_{out}}}{P_{out}} (1 - \eta_{converter}) \quad (2)$$

where the S-PPC efficiency ($\eta_{converter}$) is a function of its active power and total nonactive power (N_{total}), which also depends on the value of V_C

$$\eta_{converter} = f(P_{C_{out}}, N_{total}, V_C). \quad (3)$$

B. Voltage Step-Up/Down Operation of S-PPC Type-I

Equation (2) is valid to voltage step-up type-I S-PPC, where the value of V_C is always positive. However, the type-I can also operate as voltage step-down if the topology allows inverting the polarity of V_C . In this case, the value of $P_{C_{out}}$ is negative, which means that the power flow in the S-PPC is reversed. The power flow is represented by the arrows in Fig. 3. As can be observed, operating as voltage step-up ($V_C > 0$), the S-PPC power flow has the same direction as the direct power flow, and if the polarity of V_C is inverted ($V_C < 0$), the power flow is reversed and the S-PPC operates in voltage step-down mode.

In order to represent the overall efficiency for the case where $P_{C_{out}}$ can be positive or negative, (2) has been rewritten to the

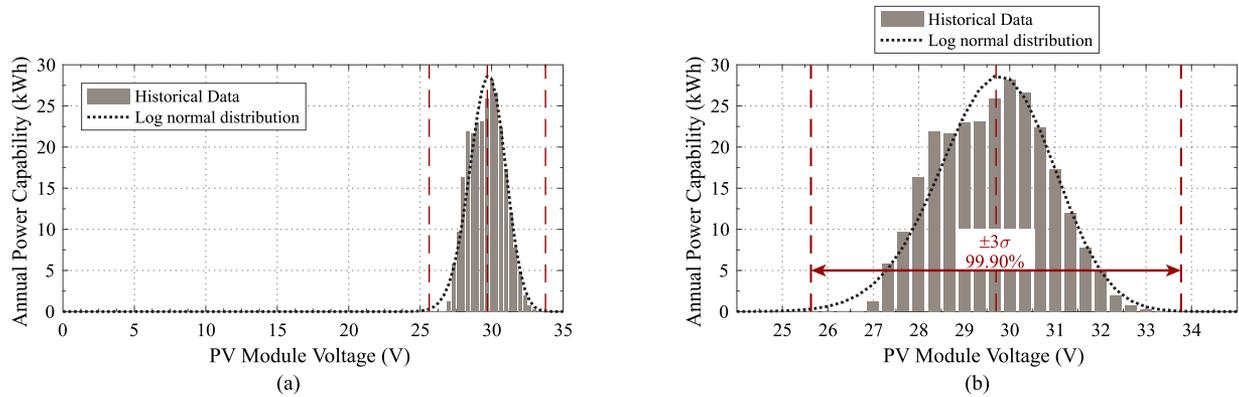


Fig. 4. Histogram of estimated annual energy production and PV module voltage level based on historical data and a log normal density distribution model for the site of São Martinho da Serra and PV module SunEarth TPB 60-P.

following:

$$\eta_{\text{global}} = \frac{P_{\text{out}}}{P_{\text{in}}} = 1 - \frac{|P_{C_{\text{out}}}|}{P_{\text{out}}} (1 - \eta_{\text{converter}}). \quad (4)$$

C. Voltage Range

The power delivered by the PV modules depends on climate conditions such as irradiation and temperature, which experiment a wide range of variation throughout the day and the year, and it depends on the PV installation site. To take these characteristics into account, the IEC 61683:1999 standard [20] and EN 50530:2010 [21] establish the concept and measurement procedures of weighted average efficiency (η_W). This figure of merit represents the power converter efficiency considering the operation at different input power levels, where the weighting coefficients of each power level are calculated based on the fraction of the power that is generated at the corresponding power range. Therefore, in order to have a good weighted average efficiency, the power converter shall be more efficient at a high weighted power level that corresponds to the power range at which more energy is generated, usually in a region close to 50% of nominal load [22].

For the S-PPC design, not only the power variations caused by climate conditions shall be considered, but also the voltage levels at which electric power is generated. The input voltage range of the S-PPC operation is very important since it defines the voltage gain required to perform MPPT on each string, and consequently the active power rating of the S-PPC.

By knowing *a priori* the solar irradiation and temperature profile of a given location, and by applying it on a PV cell model, operating at the maximum power point, it is possible to estimate the energy production and the voltage level at which it occurs. For instance, Fig. 4(a) shows a histogram with the voltage profile of energy production for a ten-year historical dataset that was collected with a minute-to-minute frequency and applied to a single exponential PV module model [23]. The data collection is from the site location of São Martinho da Serra (Brazil) measured by SONDA project from 2005 to 2014 [24] and the PV module considered is the 235 W SunEarth TPB 60-P.

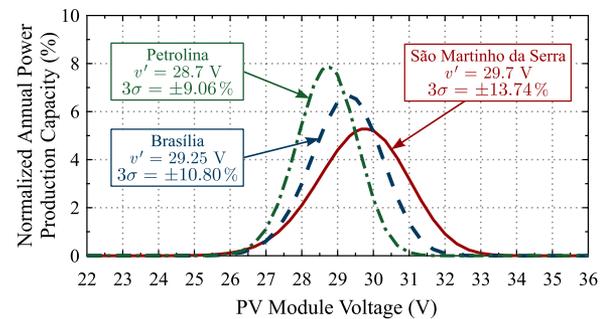


Fig. 5. Density distribution functions of three different sites in Brazil.

The statistical data are scattered in a log normal density distribution function as demonstrated in detail in Fig. 4(b). The peak energy voltage (v') calculated is 29.7 V, and the standard deviation (σ) is 1.36 V. It is observed that 99.90% of total energy is produced inside a voltage range of six standard deviations ($\pm 3\sigma$), from 25.6 to 33.8 V, which corresponds to $\pm 13.74\%$ of v' . Therefore, the voltage regulation range of the S-PPC (Δv) must be greater than 6σ in order to ensure a good energy harvesting. In this example, a definition of $\Delta v = 30\%$ of v' ($\pm 15\%$) is considered adequate.

Despite the fact that PV modules often operate at low irradiance levels, corresponding to low voltage levels at the maximum power point, Fig. 4 shows that actually a very small amount of energy is generated at those levels. Even considering that the S-PPC regulator will not be able to track the maximum power point outside the Δv range, the loss in electric power production is small compared to the converter loss reduction that can be achieved when operating inside the Δv range.

The example presented in this paper is for the site of São Martinho da Serra, but for each PV model and site installation, the values of v' and σ may be different. To demonstrate this, the voltage scattering analysis was performed for other sites of SONDA project: Brasília and Petrolina, which exhibit smaller values of v' and σ , as shown in Fig. 5. The higher the value of σ , the higher should be the definition of Δv , and the S-PPC will need to be designed for more active power.

TABLE I
NUMBER OF PV MODULES PER STRING

Operation mode	Number of PV modules
Voltage step-up	$N_{PV} \leq \frac{V_{out}}{v' + \frac{\Delta v}{2}}$
Voltage step-down	$N_{PV} \geq \frac{V_{out}}{v' - \frac{\Delta v}{2}}$
Voltage step-up/down	$N_{PV} \approx \frac{V_{out}}{v'}$

Since the dc bus voltage (V_{out}) required by the inverter is defined by the grid (around 400 V for single phase and 650 V for three-phase), and the string voltage range relies on its voltage distribution characteristics, the number of series-connected modules in a string (N_{PV}) must be properly chosen in order to minimize the voltage range required from S-PPC. The maximum operation voltage of the string ($V_{in_{max}}$) and its minimum ($V_{in_{min}}$) are calculated by the following:

$$V_{in_{max}} = \left(v' + \frac{\Delta v}{2} \right) N_{PV} \quad (5)$$

$$V_{in_{min}} = \left(v' - \frac{\Delta v}{2} \right) N_{PV}. \quad (6)$$

There are three possible operation modes of S-PPC depending on the characteristic of voltage gain of the topology: step-up, step-down, and step-up/down. For a converter connected in type-I configuration, if the S-PPC topology is step-up only (V_C always positive), the maximum N_{PV} is defined by the restriction that the string voltage cannot be greater than V_{out} . In step-down only (V_C always negative), the minimum N_{PV} must ensure that V_{in} will be always greater than V_{out} . If the S-PPC topology is designed to operate in both positive and negative values of V_C , then N_{PV} is chosen so that V_{in} is as close as possible to V_{out} . Table I presents these restrictions for calculating N_{PV} .

Considering the example where $\Delta v = 30\%$, the design of a step-up S-PPC is to have a unitary gain ($V_{in} = V_{out}$) at $V_{in_{max}}$ and its maximum voltage gain when $\frac{V_{in}}{V_{out}} = 70\%$, where $\frac{V_{in}}{V_{out}} = \frac{1}{M}$. From (1), in the worst case, the active power in the S-PPC is 30% of P_{out} , as illustrated in Fig. 6(a).

Considering the use of a step-down configuration, when $V_{in} = V_{in_{max}}$, the S-PPC active power is also 30% of P_{out} , as illustrated in Fig. 6(b).

On the other hand, using a step-up/down S-PPC topology, the number of PV modules can be designed to match the unitary voltage gain in the middle of the voltage range. It allows the output voltage of S-PPC to be reduced by half to maintain the same input voltage range, resulting in a reduction of its active power, as illustrated in Fig. 6(c), where it can be seen that the S-PPC maximum active power is only 15% in each operation mode.

In the three cases, the input voltage range is the same, but the use of step-up/down S-PPC topology actually halves the active power rating of the S-PPC. Moreover, another important characteristic is that the S-PPC active power is near zero in

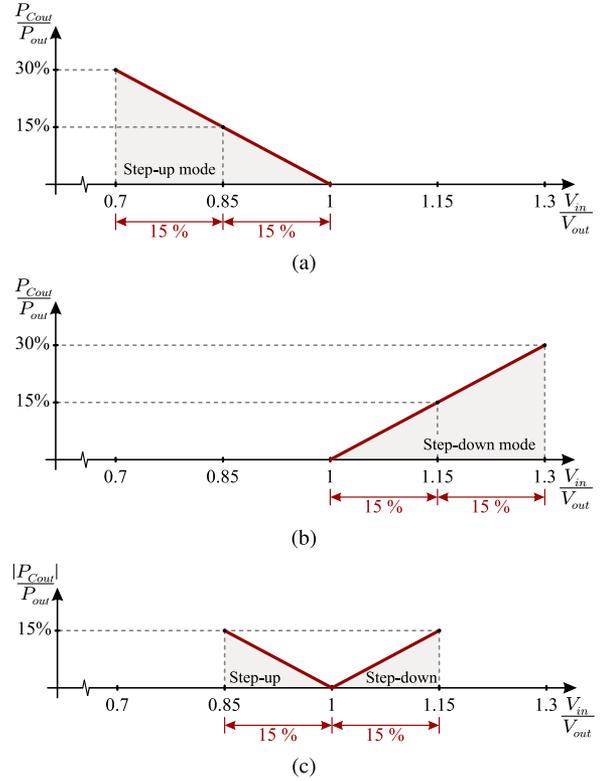


Fig. 6. Relationship between the S-PPC's active power and the total active power for: (a) step-up mode, (b) step-down mode, and (c) step-up/down modes.

the middle of the Δv range. It means that the S-PPC may have fewer losses in the voltage operation point in which most energy is generated.

III. PROCESSED ENERGY CALCULATION

The use of the S-PPC allows a significant reduction in active power compared to standard full power processing topologies. However, the series connection is not a sufficient condition to ensure partial-power processing. This is demonstrated in [14] and [15], where a case study of the buck-boost converter connected as a series regulator has demonstrated a similar performance in terms of energy processing and efficiency compared to a conventional boost converter. The same behavior happens for the flyback S-PPC topology [16].

In order for any topology to be considered with partial-power processing, it must process a smaller amount of energy in its elements than a conventional nonisolated topology operating under the same input and output conditions. Furthermore, even the topologies that present partial-power processing, for instance, forward S-PPC and full-bridge S-PPC topologies, several design parameters may affect the amount of the processed power, such as voltage regulation range, duty cycle, and transformer turns ratio.

Even topologies submitted to the same active power can present different levels of nonactive power processing. This section presents a calculation procedure of the nonactive power processed in the elements of a converter, which can be used as

an indicative to identify which topology processes more or less energy than others [15], [25].

A. Nonactive Power

In a power converter, during a switching period, the semiconductors switch the circuit configuration resulting in circulation of energy without that energy being necessarily transferred from source to load (i.e., converted into active power). In dc circuits, where the fundamental frequency of the voltage is zero, this power flow is called nonactive power, according to the definition given by IEEE Std. 1459-2010 [26], which differentiates the adopted terms for reactive and nonactive power. Nonactive power (N) is the power flow that does not result in active power at any frequency, and its unit of measure is the reactive volt-amp (var). Although this concept can be employed in ac and dc systems, nonactive power is not usually evaluated in dc-dc converters. Since the analysis of active power is not enough to ensure PPP, in this paper, the nonactive power is employed to evaluate the performance of dc-dc S-PPCs.

With the converter operating in steady state, the volt-second balance on inductor and charge balance on the capacitor results that the active power in the energy storage elements (capacitors and inductors) is ideally zero. However, the nonactive energy flowing in these elements causes losses, therefore it must be considered as an energy processed by the converter. The amount of energy that is absorbed and released in these elements during a switching period corresponds to the variation of energy in the inductor (ΔE_L) and in the capacitor (ΔE_C), calculated by (7) and (8), where d is the duty cycle and T_S is the switching period

$$\Delta E_L = \int_0^{dT_S} |v_L(t) i_L(t)| dt = \int_{dT_S}^{T_S} |v_L(t) i_L(t)| dt \quad (7)$$

$$\Delta E_C = \int_0^{dT_S} |v_C(t) i_C(t)| dt = \int_{dT_S}^{T_S} |v_C(t) i_C(t)| dt. \quad (8)$$

The nonactive energy processed by the accumulator elements ($E_{N_{\text{int}}}$) during a switching period, for n_L inductors and n_C capacitors is defined by

$$E_{N_{\text{int}}} = \sum_{j=1}^{n_L} 2\Delta E_{Lj} + \sum_{k=1}^{n_C} 2\Delta E_{Ck} \quad (9)$$

and the total nonactive power processed internally in the converter (N_{int}) is

$$N_{\text{int}} = \frac{E_{N_{\text{int}}}}{T_S}. \quad (10)$$

In addition to the nonactive power processed by the converter filters, it is also necessary to consider the nonactive power flow at input source terminals and the converter (N_{in}) and the nonactive power between the converter and load (N_{out}), which are calculated by (11) and (12) [26]

$$N_{\text{in}} = \sqrt{S_{\text{in}}^2 - P_{\text{in}}^2} \quad (11)$$

$$N_{\text{out}} = \sqrt{S_{\text{out}}^2 - P_{\text{out}}^2}. \quad (12)$$

The total nonactive power of the converter is defined as the sum of the nonactive power in the elements and the nonactive powers at input and output

$$N_{\text{total}} = N_{\text{in}} + N_{\text{int}} + N_{\text{out}}. \quad (13)$$

B. Component Stress Factor

Another evaluation methodology that can be employed to compare the stress that the components of different topologies are submitted to is the CSF, also called component load factor [27], [28]. This figure of merit represents a quantitative level of the stress level in a converter by considering the apparent power that each component of the converter is subjected to in relation to the output active power. The CSF of each component is calculated by

$$\text{CSF} = \frac{I^* V^*}{P_{\text{out}}} \quad (14)$$

and the total CSF is the sum of the value of all components.

The considered value of V^* and I^* depends on the component type. The value of V^* is the maximum blocking voltage that the element is submitted to for transistors and diodes, for capacitors the average value is considered, and for inductors and transformer windings, V^* is calculated by the average ac voltage, which is the product of applied voltage and duty cycle if a square wave excitation voltage is assumed [27]. On the other hand, the value of I^* is the rms current for MOSFETs, inductors, transformers, and capacitors. For IGBTs and diodes, the average current value is chosen.

In [4], the total CSF was calculated for four different topologies: a standard full-power boost; a buck-boost S-PPC; a full-bridge S-PPC; and a push-pull S-PPC. The results show that the buck-boost S-PPC presented the same performance as the standard full-power boost and the full-bridge S-PPC, and the push-pull S-PPC featured lower CSF values in comparison to the standard full-power boost, indicating that S-PPCs can perform better compared to the standard full-power converters. In order to expand the analysis presented in [4], the same CSF calculation methodology is also employed in this paper for the full-bridge and FB/PP S-PPC topologies, whose results are presented in Section IV.

IV. COMPARISON BETWEEN STEP-UP S-PPC AND STEP-UP/DOWN S-PPC TOPOLOGIES

In order to compare the use of a voltage step-up S-PPC to a voltage step-up/down S-PPC topology, this section presents the performance analysis of full-bridge dc-dc S-PPC topology and a FB/PP S-PPC topology.

A. Full-Bridge S-PPC Topology (FB S-PPC)

The full-bridge topology (labeled as FB S-PPC), whose schematics is illustrated in Fig. 7, is largely known in technical literature as having a good performance in terms of efficiency and power density. The primary switches are phase-shift modulated, whereas the secondary diodes act as a passive rectifier with an LC filter. Since in this topology the voltage V_C

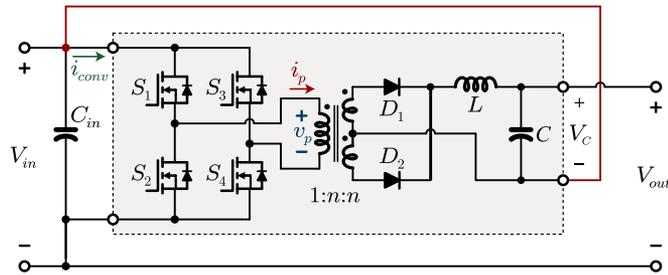


Fig. 7. Full-bridge S-PPC topology schematics (labeled as FB S-PPC).

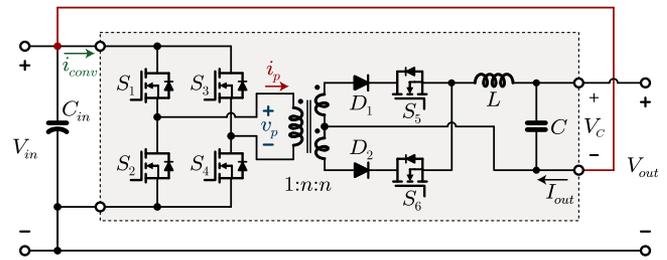


Fig. 9. Full-bridge/Push-pull S-PPC topology schematics (labeled as FB/PP S-PPC).

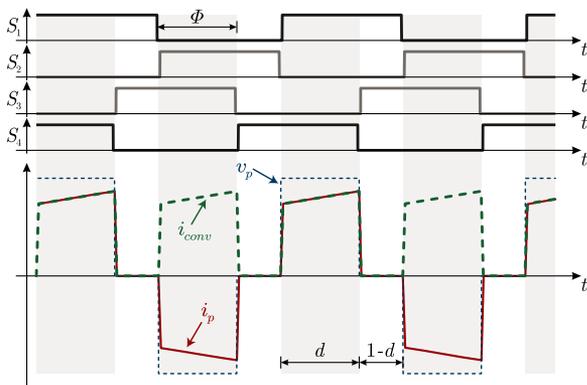


Fig. 8. Switching sequence for Full-bridge S-PPC topology.

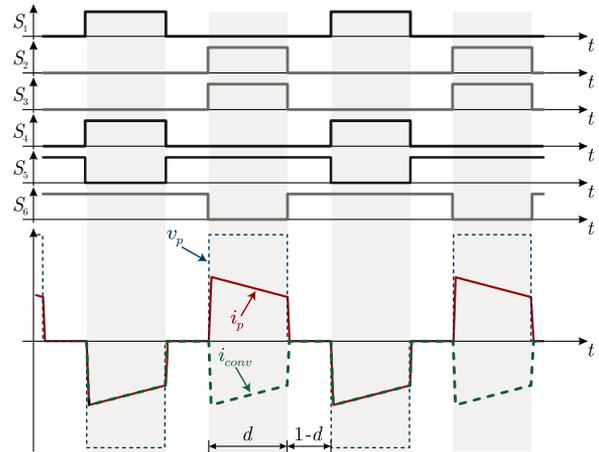


Fig. 10. Switching sequence for FB/PP S-PPC operating in voltage step-down mode.

is always positive, the S-PPC is voltage step-up. In addition, it can be designed to operate with ZVS on the primary bridge for a certain load current range. The switching sequence of the FB S-PPC and the waveforms of voltage and current across the primary transformer winding and the S-PPC input current (i_{conv}) are presented in Fig. 8.

B. Full-Bridge/Push-Pull S-PPC Topology (FB/PP S-PPC)

For operation as a voltage step-up/down regulator, the topology employed as S-PPC must be bidirectional. Considering the type-I configuration, in order to operate as step-down, the S-PPC must invert the power flow by inverting the polarity of its output voltage (V_C) and its input current (i_{conv}). It sets the requirements to a type-I S-PPC topology to operate as a voltage step-up/down regulator: the topology must have bidirectional input current and bidirectional output voltage. It means that any topology that fits these requirements can be employed.

In the comparison presented in this paper, the full-bridge/push-pull S-PPC topology (labeled as FB/PP S-PPC) shown in Fig. 9 [29] is employed, which is derived from the FB S-PPC and a current feed push-pull. When connected as a type-I S-PPC, this topology can operate in two distinct modes: as a full-bridge with $V_C > 0$, or as a reversed current feed push-pull with $V_C < 0$.

In voltage step-up operation mode, switches S_1 to S_4 are phase-shift modulated in order to control the voltage V_C similarly to the FB S-PPC (see Fig. 8), while switches S_5 and S_6 are

constantly turned-ON. In this operation mode, the FB/PP S-PPC behaves like an FB S-PPC.

In voltage step-down operation mode (push-pull), the energy flow in the FB/PP is inverted and the converter can be seen as having its input source in V_C . In this case, S_5 and S_6 operate as the primary of a current feed push-pull, and the bridge formed by S_1 to S_4 acts as a rectifier pushing power back to the source V_{in} . The output current flow I_{out} causes the voltage V_C to have its polarity reversed, being controlled by switches S_5 and S_6 . While S_5 and S_6 are both turned ON, the secondary circuit acts as a magnetic short, charging the inductor. When S_5 or S_6 are turned OFF, the inductor current is driven to primary, making the S-PPC input current (i_{conv}) negative. The value of d in this mode of operation is considered as the time interval in which S_5 or S_6 are OFF, and $1 - d$ is the time interval in which both are conducting.

Operating as push-pull, switches S_1 to S_4 are synchronously controlled to the modulation of S_5 and S_6 to form an active rectifier. The waveforms of voltage and current across the primary transformer winding and the S-PPC input current (i_{conv}) and the switching sequence of the FB/PP operating in the voltage step-down mode with active rectification are presented in Fig. 10. As can be seen, the current i_{conv} is negative in this operation mode.

Based on numerical simulations, a comparative analysis is carried out, evaluating the two topologies with respect to their nonactive processed power and CSF. The simulations have been

TABLE II
DESIGN EXAMPLE SPECIFICATIONS

Parameter	FB S-PPC	FB/PP S-PPC
Input voltage (V_{in})	154–220 V	187–253 V
Input voltage range (Δv)	66 V (30%)	66 V (30%)
Output voltage (V_{out})	220 V	220 V
Maximum S-PPC active power ($P_{C_{out}}$)	225 W	112.5 W
Output active power (P_{out})	750 W	750 W
Switching frequency (f_s)	35 kHz	35 kHz
Inductor current ripple (Δi_L peak)	10%	10%
Output voltage ripple ($\Delta v_{C_{out}}$ peak)	1%	1%
Simulation time step (T_{step})	1.74386 ns	1.74386 ns

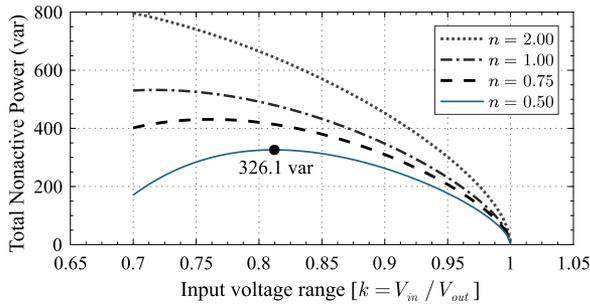


Fig. 11. Total nonactive power in FB S-PPC for different values of transformer turns ratio ($n = N_S / N_P$).

performed in MATLAB software, employing state-space mathematical models considering lossless circuit (ideal components) and using the calculation procedure presented in Section III for a design example with reduced scale, whose parameters are presented in Table II. In the analysis, the load is fixed at 750 W, and the difference between the input and output voltage ($k = 1/M = V_{in}/V_{out}$) is varied from 0.7 to 1.0 for the FB S-PPC and from 0.85 to 1.15 for the FB/PP S-PPC, resulting in an input voltage range of 66 V (30% of V_{out}) in both converters.

C. Full-Bridge S-PPC Analysis

The calculated values of total nonactive power in the FB S-PPC are shown in Fig. 11, considering different values of transformer turns ratio $n = N_S / N_P$, where N_P is the number of turns on the primary winding and N_S is the number of turns of each secondary winding. It is observed that the nonactive power processed in the circuit is lower as k approaches one. Also, the use of smaller values of n results in lower values of nonactive power, indicating that the lower the turns ratio in the transformer, the smaller the amount of power processed.

However, the minimum value of the transformer turns ratio is limited by the maximum duty cycle (d_{max}). Since the static gain of the full-bridge converter is calculated as $V_C / V_{in} = nd$, where d is the duty cycle ranging from 0 to 100% corresponding to 0° to 180° on the phase-shift (Φ) between the full-bridge arms, then the minimum value of n can be obtained by

$$n_{min} = \frac{V_{C_{max}}}{V_{in_{min}} d_{max}} = \frac{V_{out} - V_{in_{min}}}{V_{in_{min}} d_{max}}. \quad (15)$$

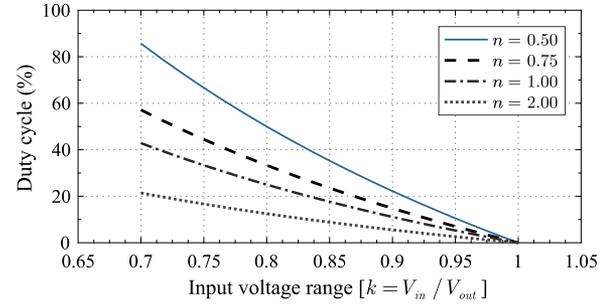


Fig. 12. Full-bridge S-PPC duty cycle for different values of n .

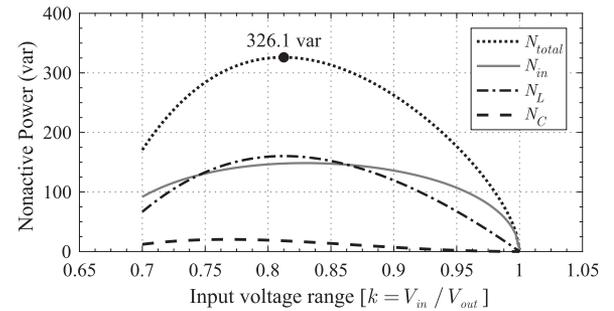


Fig. 13. Detail of nonactive power in the components of the full-bridge S-PPC with $n = 0.5$.

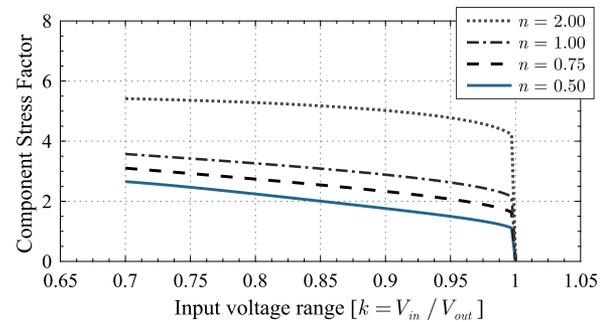
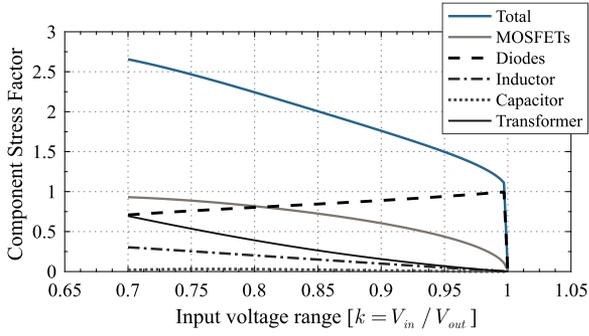
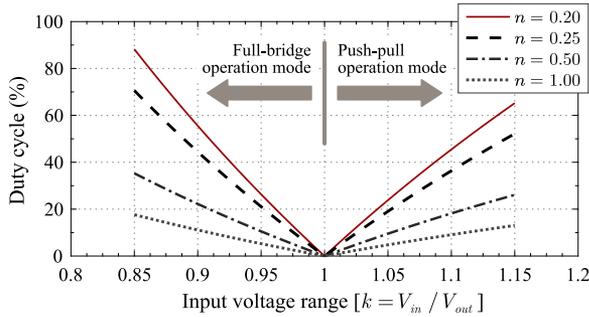


Fig. 14. Total CSF on the FB S-PPC topology for different values of n .

In this example, $n = 0.5$ is considered an adequate choice, since it corresponds to a d_{max} of 85.7%, leaving a margin of 14.3% left for control action, nonmodeled losses, dead time, etc. The duty cycle values for different values of n are shown in Fig. 12.

Fig. 13 presents the values of nonactive power processed by the inductor (N_L), by the capacitor (N_C), by the input source (N_{in}), and total nonactive power (N_{total}) considering $n = 0.5$. In this example, the load is considered purely resistive, so the output nonactive power is zero.

The calculated values of CSF for the FB S-PPC topology with different values of n are presented in Fig. 14. Similarly as it happens to the nonactive power, the CSF is also reduced with the reduction of n .


 Fig. 15. Individual CSF values for FB S-PPC with $n = 0.5$.

 Fig. 16. FB/PP S-PPC duty cycle for different values of n .

Considering $n = 0.5$, the total CSF values and those for each element of the FB S-PPC are shown in Fig. 15. These results are consistent with the results obtained in [4].

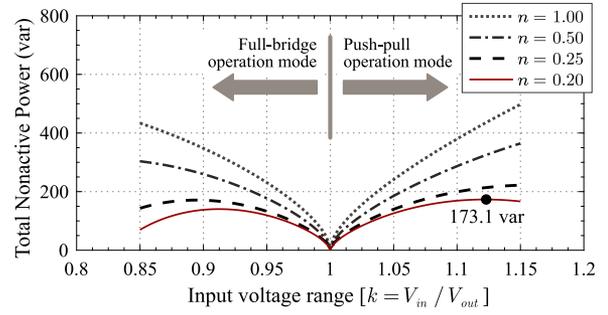
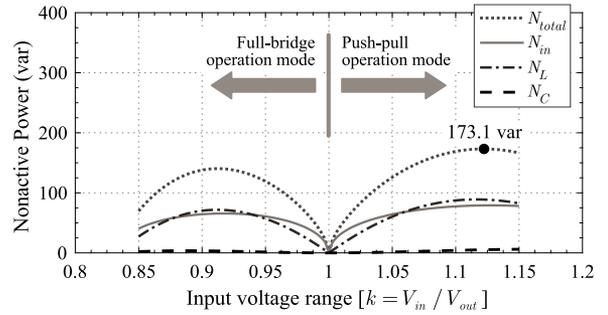
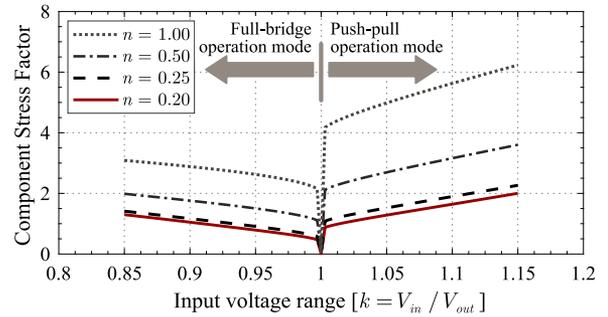
D. FB/PP S-PPC Analysis

Although the value of Δv is the same as in the FB S-PPC topology, the FB/PP S-PPC operates with v_C from 0 to $\frac{\Delta v}{2}$ in full-bridge mode, and from 0 to $-\frac{\Delta v}{2}$ in push-pull mode, allowing the use of smaller values of n , as can be seen in Fig. 16. The minimum transformer turns ratio is also limited by d_{\max} , which occurs in voltage step-up mode. In the design example, applying (15), the use of $n = 0.2$ is considered an appropriate choice, resulting in d_{\max} of 88.3% in full-bridge operation mode and 66.3% in the push-pull operation mode.

In both modes of operation, nonactive power is reduced with small values of n , as shown in Fig. 17. When the input voltage is equal to the output voltage ($k = 1$), the duty cycle is zero. At this exact point of operation, there is no power processing and there are only conduction losses on the circuit.

Considering $n = 0.2$, the values of nonactive power in the inductor, capacitor, input source, and total nonactive power are presented in Fig. 18. Although the S-PPC operates at a lower d in push-pull operation mode, the amount of energy processed by the elements is higher, resulting in higher levels of nonactive power.

It is observed that the values of nonactive power processed in the elements of the FB/PP S-PPC with $n = 0.2$ are smaller when compared to the values obtained for the FB S-PPC with


 Fig. 17. Total nonactive power in FB/PP S-PPC for different values of n .

 Fig. 18. Detail of nonactive power in the components of the FB/PP S-PPC with $n = 0.2$.

 Fig. 19. Total CSF on the FB/PP S-PPC topology for different values of n .

$n = 0.5$, reducing 46.9% from 326.1 to 173.1 var in the worst case.

The values of total CSF for the FB/PP S-PPC topology with different values of n are presented in Fig. 19. It is observed that in the middle of the voltage range, when k is near 1, the CSF is smaller than in the input voltage extremes.

The total CSF values in each element of the FB/PP S-PPC are shown in Fig. 20. As well as the nonactive power, the values of CSF are greater in push-pull operating mode, caused mainly by switches stresses.

E. Analysis of Nonactive Power Considering Different Values of Δv

In order to evaluate the behavior of nonactive power for different values of Δv , this section presents simulation results for the same topologies presented before, with the same parameters,

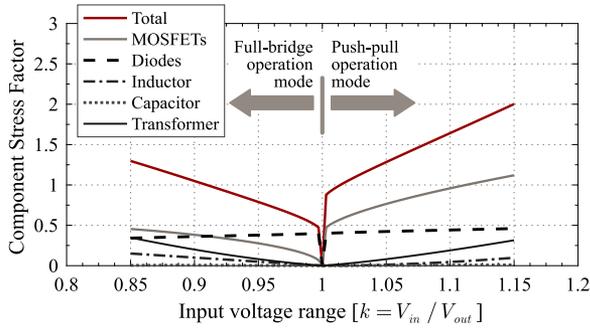


Fig. 20. Individual CSF values for FB/PP S-PPC with $n = 0.2$.

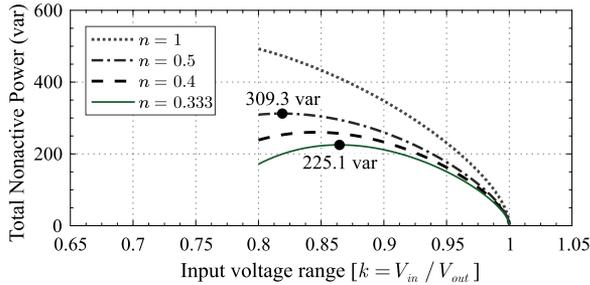


Fig. 21. Nonactive power in full-bridge step-up S-PPC considering $\Delta v = \pm 10\%$ for different values of n .

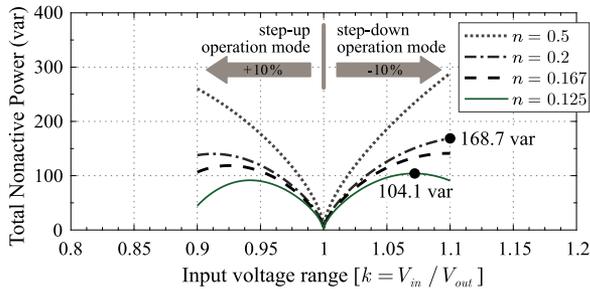


Fig. 22. Nonactive power in FB/PP step-up/down S-PPC considering $\Delta v = \pm 10\%$ for different values of n .

except the definition of Δv , which was reduced from 30% to 20% of v' .

Considering the step-up FB S-PPC topology, a range of 20% results on a $V_{C_{max}} = 44$ V and $P_{C_{out}} = 20\%$ of P_{out} . As seen in Fig. 21, maintaining the same turns ratio of the example design ($n = 0.5$), it results in a small reduction in nonactive power (from 326.1 to 309.3 var). However, the smaller voltage gain required by the FB S-PPC allows to reduce the turns ratio to 1/3 (0.333), and this makes the total nonactive power to be reduced to 225.1 var in the worst case.

The same behavior can be observed for step-up/down topologies. In the case of FB/PP S-PPC, the definition of $\Delta v = 20\%$ ($\pm 10\%$) allows a reduction of $P_{C_{out}}$ to only 10% of P_{out} . Also, the small Δv allows reducing the turns ratio to 1/8 (0.125) and the nonactive power to only 104.1 var in the worst case, as presented in Fig. 22.

TABLE III
PROTOTYPES PARAMETERS

Part	FB S-PPC	FB/PP S-PPC
Output capacitor (C)	352 μ F	352 μ F
Inductor value (L)	198 μ H	240.5 μ H
Inductor core	Magnetics 77930	Magnetics 77930
Inductor turns	51 turns	62 turns
Inductor copper wire	10 \times 27 AWG	10 \times 27 AWG
Transformer ferrite	IP6 NEE-42/42/15	IP6 NEE-30/30/14
Transformer windings	34 / 17 / 17 turns	35 / 7 / 7 turns
Primary MOSFETs	IRFP360LC	IRFP360LC
Secondary MOSFETs	—	IPP220N25NFD
Secondary Diodes	SDT12S60	MBRF10200CT

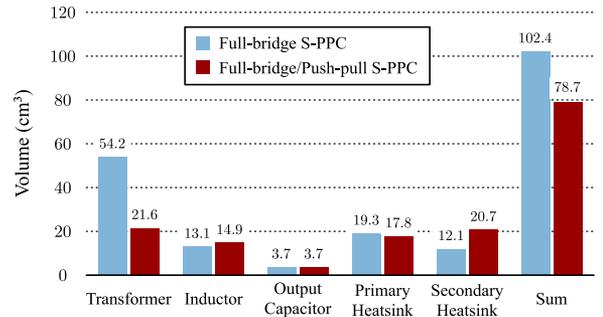


Fig. 23. Volume of components of the two prototypes.

This analysis shows that the value of Δv is one of the most important parameters of the design of S-PPC converters since it affects not only the active power but also the nonactive power processing. In addition, the analysis demonstrates that a reduction of Δv is not enough to reduce the nonactive power: the value of n must be optimized to obtain the best system performance for each project.

In the design of S-PPC converters, the definition of large values of Δv can be useful when the voltage profile generated by the panels in that locality is not known in detail and can be installed in different locations and different panel technologies. On the other hand, knowing the voltage profile of a particular PV module model and the location where it is being installed, it is possible to optimize the value of Δv to minimize the power processing on the S-PPC and its power losses.

V. EXPERIMENTAL RESULTS

In order to validate the theoretical analysis, a prototype of the FB S-PPC topology with $n = 0.5$ and a prototype of the FB/PP S-PPC topology with $n = 0.2$, both with $\Delta v = 30\%$, were implemented and submitted to experiments. To have a fair comparison between the two topologies, the main parameters (V_{out} , P_{out} , f_s , $\Delta v_{C_{out}}$, and Δi_L) are equal in both the prototypes. These parameters are the same as those of the simulations presented in Table II. However, since the FB/PP S-PPC topology presents lower active power, more components, and two modes of operation, the components must be sized for the worst case of operation, resulting in different sizes in magnetics and heatsinks. The practical parameters of the two prototypes are presented in Table III.

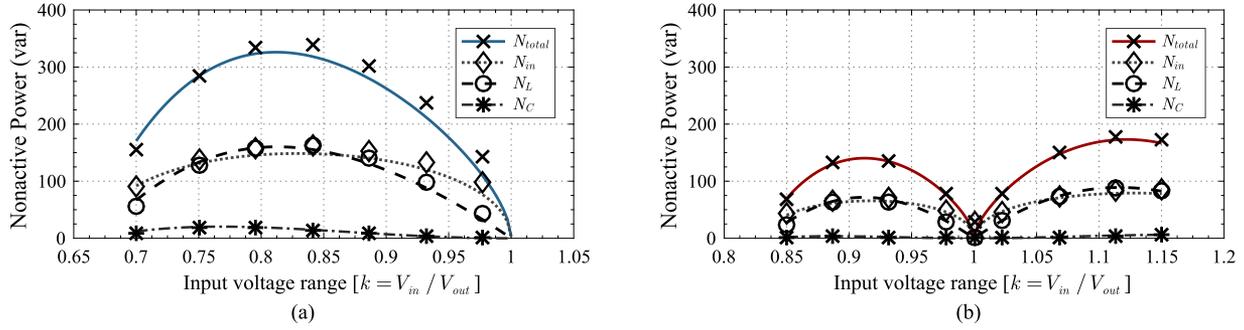


Fig. 24. Experimental results of nonactive power, where lines correspond to the simulated values and markers correspond to the data obtained experimentally. (a) For the FB S-PPC prototype; (b) For the FB/PP S-PPC prototype.

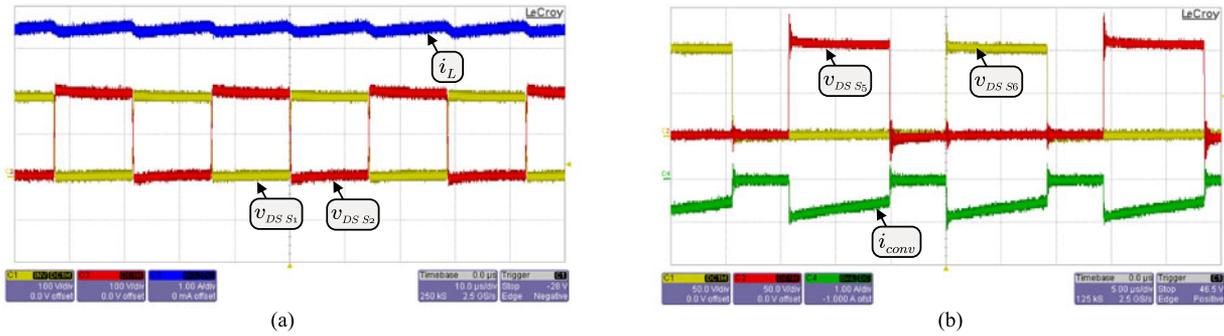


Fig. 25. FB/PP S-PPC experimental waveforms. (a) Operation in step-up mode ($v_{in} = 187$ V); inductor current (blue, 1 A/div) and voltages across primary MOSFETs (red and yellow, 100 V/div). (b) Operation in step-down mode ($v_{in} = 253$ V); converter input current (green, 1 A/div) and voltages across secondary MOSFETs (red and yellow, 50 V/div).

TABLE IV
PROTOTYPES POWER DENSITY COMPARISON

	FB S-PPC	FB/PP S-PPC
Total components volume	204.8 cm ³	157.4 cm ³
Overall power density (ρ)	3.66 W/cm ³	4.76 W/cm ³

The volume of components employed in each prototype is shown in Fig. 23. It is observed that although the active power in the FB/PP S-PPC is half as in the FB S-PPC, this does not result in the same volume reduction of its elements. It occurs because the FB/PP S-PPC has more switching elements and its components must be sized for the worst case of operation in both operation modes. Nevertheless, it is observed that the sum of the volume occupied by the components of the voltage step-up/down topology is about 23.4% smaller than in the voltage step-up topology, allowing a significant increase in the power density of the system.

The overall power density (ρ) is defined as the division of the power output (P_{out}) by the total volume, where the total volume is typically a factor of two more than the sum of the partial volumes [30]. Table IV presents the power density of the two prototypes.

The experimental values of the nonactive power processed by the prototypes are obtained from the voltage and current

waveforms measured at the input and output terminals of the converter, as well as in the storage elements (inductors and capacitors). The values of nonactive power for all input voltage range are shown in Fig. 24(a) for the FB S-PPC prototype and in Fig. 24(b) for the FB/PP S-PPC prototype, where lines correspond to the simulated values and markers correspond to the data obtained experimentally. It is observed that the values obtained experimentally are in agreement with the values of the numerical simulation, validating the proposed analysis.

Aiming to validate the operation of the FB/PP S-PPC, Fig. 25(a) presents experimental waveforms of inductor current and voltage across the primary switches of the prototype operating in voltage step-up mode (with $v_{in} = 187$ V). Fig. 25(b) presents waveforms of S-PPC input current and voltage across the secondary MOSFETs of the FB/PP S-PPC prototype operating in step-down mode (with $v_{in} = 253$ V). In these figures, it can be observed that the oscillations caused by the resonance of parasitic elements of the converter during switching, which are not considered by the models, result in extra nonactive power circulation, justifying the small error between the simulated values and those obtained experimentally.

Active power and efficiency have been measured by a *Yokogawa* WT1800 precision power meter, considering only the power stage. Fig. 26 shows the measurement of the FB/PP S-PPC prototype operating at the point $k = 0.85$. The efficiency curves obtained for the entire input voltage range measured at the S-PPCs input/output terminals are presented in Fig. 27(a),

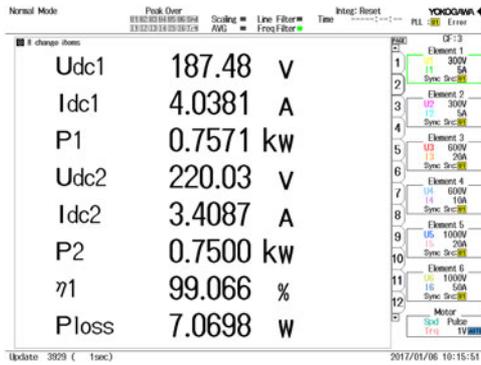


Fig. 26. Power and efficiency measurement of FB/PP S-PPC with $V_{in} = 187$ V ($k = 0.85$).

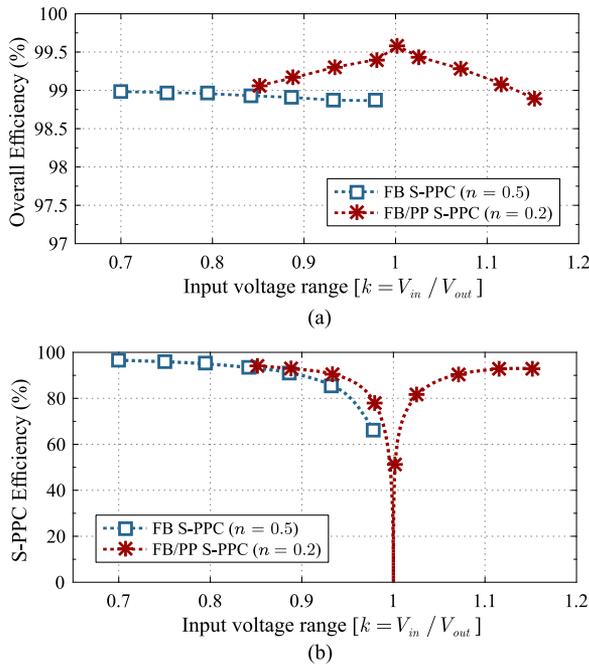


Fig. 27. Measured efficiency of the two prototypes. (a) Measured efficiency on the S-PPC terminals and (b) overall efficiency measured in the input and output of the dc–dc stage.

and the overall efficiency curves of the dc–dc stage at rated power are presented in Fig. 27(b). As it can be observed, these results are in accordance with (4) and, despite the fact that the efficiency in the FB/PP S-PPC terminals is lower, its overall efficiency is higher than in the FB S-PPC.

As can be seen in Fig. 27(b), the overall efficiency of the FB S-PPC is almost flat around 98.9% throughout the entire voltage range, while the overall efficiency of the FB/PP S-PPC is higher in the center of the range ($k = 1$), reaching a maximum efficiency of 99.58%.

VI. CONCLUSION

A novel design approach for series-connected partial-power processing converters applied to string/multistring PV systems is presented in this paper. The proposed design procedure allows minimizing power processing by means of the proper choice of

the step-up/down voltage regulation range of the S-PPC, based on the voltage profile of the maximum electric power produced by the PV modules.

The employment of a voltage step-up/down topology (FB/PP S-PPC) is compared to a voltage step-up S-PPC topology (FB S-PPC) and an analysis of nonactive power and CSF is performed, indicating that the voltage step-up/down topology allows to reduce significantly the active and nonactive power, presenting less stress on its components than the voltage step-up topology. One of the main advantages of the voltage step-up/down topologies is that the minimum power processing occurs at the voltage operating point at which the most energy is generated, improving the efficiency and the power yield of the PV system.

In order to validate the proposed approach, two 750-W prototypes were implemented and tested. The FB/PP S-PPC prototype presented 46.9% lower nonactive power processing and has 23.4% lower volume compared to the FB S-PPC prototype, resulting in higher efficiency and power density.

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