Robust Design of Control Structure for Three-Phase Grid-Tied Inverters

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***Abstract*—Grid-tied inverters are being widely used in distributed generation, as in photovoltaic generation. This paper presents the robust design and analysis of a control structure for three-phase grid-tied inverters based on stationary frame. The synchronization with the grid is carried out using a DMSOGI-FLL structure, which allows to estimate DC offset voltage and it increases the system robustness under grid voltage abnormalities. Furthermore, a current reference generator is detailed considering the dc-link voltage regulation and the control of active and reactive power. A proportional resonant (PR) approach with harmonic compensation (HC) is applied for the output inverter current control. Moreover, the proposed structure also includes an active damping technique with capacitor current estimation to improve the system robustness in weak or strong grids. Results under several operating conditions are presented from a numerical analysis and it demonstrates the performance of the proposed control structure.**

***Index Terms*—Resonant controller, Active damping, Grid-connected converters.**

I. Introduction

The increases of distributed generation (DG) systems connected in main grid led to intense research in order to promote the solution to the problems that appear in these systems, as instability and detection of disturbances. Moreover, the DG systems has been applied to supply the growing energy demand, mitigate the impacts caused by fossil fuel electric power generation and provide energy to isolated regions [1].

A DG system is typically connected to the main grid by single- or three-phase voltage-source inverter (VSI). However, the connection requirements need to be met in order to ensure the safety and quality of the energy injected to the grid [2–5]. Therefore, the VSI is connected to the grid by a low-pass filter to reduce and limit the switching harmonics. Moreover, the control structure of DG needs to be able to deal with abnormal grid conditions in terms of voltage and frequency deviations, and islanding situations [5].

Several control structures for DG systems are presented in literature [6–10]. However, the literature lacks a general and further analysis about control system as a whole. In this context, the main contribution of this paper is present and detail a control structure design based on stationary frame for grid connection of three-phase inverters. The design is carried out in order to increase the stability of the system in a wide range of grid parameters. Furthermore, the stability and performance results of the proposed controller are analyzed and shown in several operating scenarios.

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This paper is organized as follows: Section II shown the system that will be analyzed; Section III presents and describes the control structure composed by PLL (Phase Locked Loop), current reference generator, current control and active damping; Section IV analyses the results obtained; finally the Section V present the conclusions.

II. System Description

The DG system proposed in this paper and its parameters are presented in Fig. 1 and Table I respectively. This system is composed of a three-phase VSI, an LCL filter, local load and DC bus. The diagram also presents the control structure block that is implemented in DSP and contains the grid synchronization algorithm (PLL), current reference generator (RG) and the current control based on Proportional Resonant controller with Harmonic Compensation (PR+HC), as detailed in Fig. 2. In addition, the DC-link voltage, the converter current and the voltage of PCC (Point of Commom Coupling) are measured in order to implement the power and current control and synchronize the voltage of converter with the AC grid.

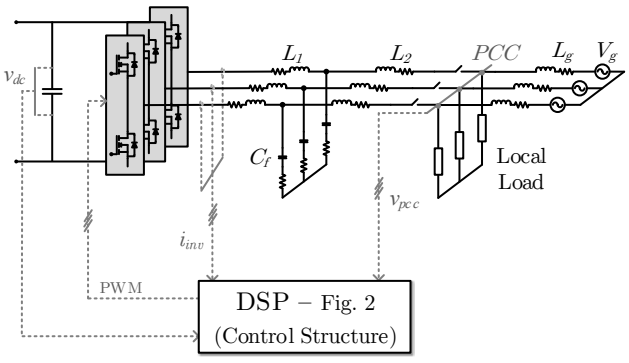


Fig. 1. Three-phase grid-tied inverter with LCL filter and DSP control.

The system state space model is given by (1-3), including LCL filter, local load and grid parameters.

$$\dot{x} = Ax + Bu, \tag{1}$$

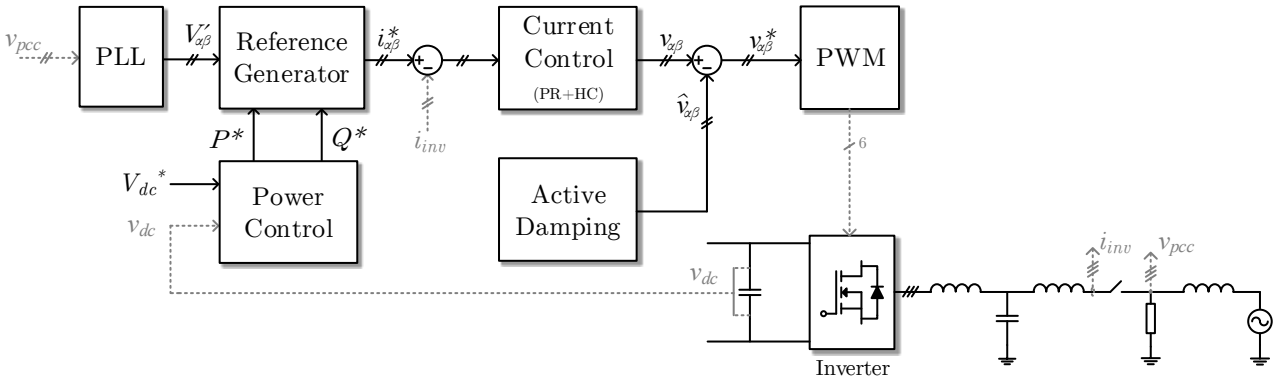


Fig. 2. Control structure for three-phase grid-tied inverter.

$$A = \begin{bmatrix} -c_1 & R_{cf}/L_1 & -1/L_1 & 0 \\ R_{cf}/L_2 & -c_2 & 1/L_2 & R_{Load}/L_2 \\ 1/C_f & -1/C_f & 0 & 0 \\ 0 & R_{Load}/L_g & 0 & -c_3 \end{bmatrix}, \quad (2)$$

$$B = \begin{bmatrix} 1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/L_g \end{bmatrix}^T. \quad (3)$$

where $x = \begin{bmatrix} i_{L1} & i_{L2} & v_{Cf} & i_g \end{bmatrix}^T$, $u = \begin{bmatrix} V_u & V_g \end{bmatrix}$, $c_1 = (R_{L1} + R_{Cf})/L_1$, $c_2 = (R_{Load} + R_{Cf} + R_{L2})/L_2$, $c_3 = (R_{Load} + R_g)/L_g$.

TABLE I
SYSTEM PARAMETERS

Parameters	Description	Value
L_1	Inverter side LCL filter inductance	100 μH
L_2	Grid side LCL filter inductance	12 μH
R_L	Inverter side LCL filter series resistance	5 mΩ
C_f	LCL filter capacitance	22 μF
R_{Cf}	LCL filter capacitor series resistance	1 mΩ
L_r	Grid equivalent inductance	2940 μH
R_g	Grid equivalent resistance	20 mΩ
V_g	Grid voltage	220 V_{rms}
R_{Load}	Local load resistance	3.23 Ω
P_{inv}	Local load power @ 220 V	15 kW
f	Grid frequency	60 Hz
f_{sw}	Switching frequency	30.72 kHz
v_{dc}	DC bus voltage	400 V

The converter is designed to 15 kW nominal power and the connection with AC mains at 220 V_{rms} and 60 Hz. Considering the connection voltage, the DC-link need to provide a minimum voltage of 311 V ($220\sqrt{2}$ V). However, due to realistic factors as the limited duty cycle of switches, DC-link voltage was chosen V_{dc} = 400 V.

III. CONTROL STRUCTURE

The control structure for the system is presented in Fig. 2. This approach is used to regulate the DC-link voltage and control the injected power in the main grid. The synchronization of the converter to the grid is implemented by a PLL, which generates the reference voltages ($V'_{\alpha\beta}$) from grid voltage (v_{pcc}), where v_{pcc} is the Clarke transformation voltages (4) from v_a, v_b and v_c. Both grid voltage and inverter current (i_{inv}) are measured and transformed from natural frame ($abc\angle 120^o$) to stationary frame ($\alpha\beta\angle 90^o$).

$$v_{pcc} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (4)$$

In Fig.2, the reference voltages are obtained using the PLL. From this voltages, the Reference Generator returns the reference current ($i^*_{\alpha\beta}$) taking into account the DC-link voltage (v_{dc}) regulation, that is carried out by the Power Control block. From the reference current and the inverter current, the Current Controller generates the control voltages ($v_{\alpha\beta}$) that are decreased by ($\hat{v}_{\alpha\beta}$), obtained from the Active Damping block. Together, those blocks generate the reference voltages ($v^*_{\alpha\beta}$) that are converted to PWM signals. The following subsections will describe and analyze these control elements individually.

A. Grid synchronization strategy

Usually a PLL algorithm is used to synchronize the converter voltage with the grid. Many techniques of PLL are discussed in literature [4], [11]. In this paper the DMSOGI-FLL (Dual Modified Second Order Generalized Integrator - Frequency-Locked Loop) is chosen due to its performance under unbalanced voltages, the frequency detection does not present high oscillations and it eliminates possible dc levels of sensors.

The DMSOGI-FLL is based on MSOGI presented in Fig. 3 for one signal of stationary reference. The MSOGI is a Modified-SOGI [6], [12], [13], that eliminates possible dc levels from sensors and auto-adapt the estimated frequency ($\hat{\omega}$) of the SOGI to the input frequency (ω_{ff}). This structure produce two in-quadrature voltages V'_α and qV'_α from v_α. The error ($K_e\varepsilon_v$) generated in Fig. 3 is described by the equation:

$$\text{SOGI}(s) = \frac{V'_\alpha}{K_e\varepsilon_v}(s) = \frac{\hat{\omega}s}{s^2 + \hat{\omega}^2}. \quad (5)$$

This way, the structure defined by (5) provide an infinite gain at the resonance frequency ($s = j\omega$) and allow the reduction of the steady-state error between the input voltage (v_α) and the output voltage (V'_α). Therefore, it is ensured that the reference voltage (V'_α) will converge to the input

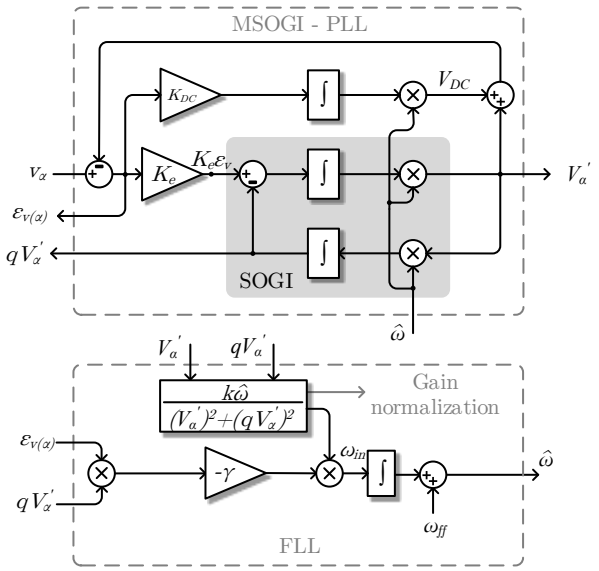


Fig. 3. Structure of the MSOGI-FLL.

voltage when the estimated frequency ($\hat{\omega}$) converges to the grid frequency (ω_{ff}). Fig. 4 presents the frequency response of (5) and it shows the attenuation of signals for a range of $\hat{\omega}$.

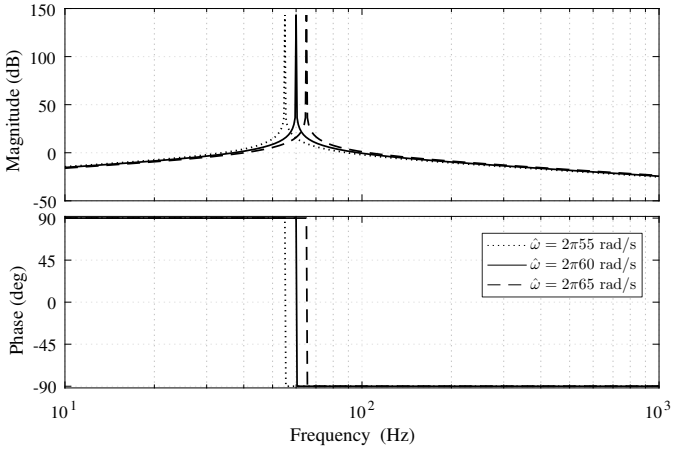


Fig. 4. Frequency response of $SOGI(s)$ at the estimated frequency $\hat{\omega}$ for 55, 60 and 65 Hz.

From Fig. 3 the voltages $V_\alpha^{'}$, $qV_\alpha^{'}$ and V_{dc} are obtained, described by:

$$\frac{V_\alpha^{'}(s)}{v_\alpha(s)} = \frac{K_e\omega s^2}{s^3 + (K_e + K_{DC})\omega s^2 + \omega^2 s + K_{DC}\omega^3}, \quad (6)$$

$$\frac{qV_\alpha^{'}(s)}{v_\alpha(s)} = \frac{K_e\omega^2 s}{s^3 + (K_e + K_{DC})\omega s^2 + \omega^2 s + K_{DC}\omega^3}, \quad (7)$$

$$\frac{V_{DC}(s)}{v_\alpha(s)} = \frac{K_{DC}\omega(s^2 + \omega^2)}{s^3 + (K_e + K_{DC})\omega s^2 + \omega^2 s + K_{DC}\omega^3}. \quad (8)$$

The frequency response analysis of (6) is shown in Fig. 5 and it demonstrates the frequency depending of a MSOGI structure for K_e values. This behavior is also observed for (7) and (8).

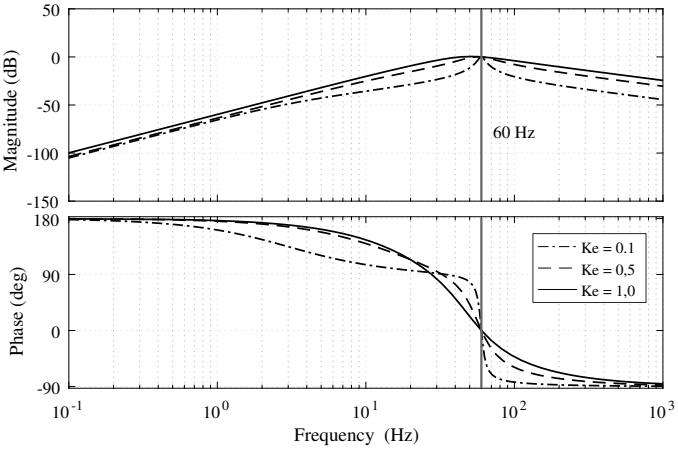


Fig. 5. Frequency response of (6) for K_e variations.

The gains K_e and γ are designed as in [14], considering the settling times in the detection of the voltage ($t_{s_{SOGI}}$) and frequency ($t_{s_{FLL}}$) inputs. Once that is recommended the $t_{s_{FLL}} \geq 2t_{s_{SOGI}}$ [15], and the standard IEEE-1547 [5] require the disconnection of the inverter to abnormal conditions of voltage and frequency in 160 ms for critical scenarios, $t_{s_{SOGI}}$ are set to 24.4 ms and $t_{s_{FLL}}$ as 150 ms.

$$K_e = \frac{9.2}{t_{s_{SOGI}}\omega} = 1.0 \quad (9)$$

$$\gamma = \frac{4.6}{t_{s_{FLL}}} = 30.667 \quad (10)$$

Therefore, the gain of SOGI to $K_e = 1.0$. The FLL is design with $\gamma = 30.667$, which provide a settling time of $t_{s_{FLL}} = 150$ ms. The grid frequency is ω_{ff} = $2\pi60$ rad/s.

In three-phase systems the DMSOGI is composed by two MSOGI structures and PNSC (Positive-Negative Sequence Calculation) block as shown in Fig. 6 [15]. The PNSC computes the sequence components on the $\alpha\beta$ reference frame according to

$$V_\alpha^{+'} = \frac{V_\alpha^{'} - qV_\beta^{'}}{2}; V_\beta^{+'} = \frac{V_\beta^{'} + qV_\alpha^{'}}{2} \quad (11)$$

$$V_\alpha^{-'} = \frac{V_\alpha^{'} + qV_\beta^{'}}{2}; V_\beta^{-'} = \frac{-qV_\alpha^{'} + V_\beta^{'}}{2}. \quad (12)$$

These components will be used in the FLL block and to generate de reference currents.

B. DC-link voltage control and reference current generator

The reference currents are generated by DC voltage control and Reference Generator [14] shown in Fig. 7. The dc-link controller modifies the active power reference including DC regulation. The DC-link voltage (v_{dc}) is filtered using a low pass filter (LFP) and then it is controlled by a PI (Proportional Integral) controller, which generates the dc regulation current. This current is multiplied by the reference voltage (V_{dc}^*)

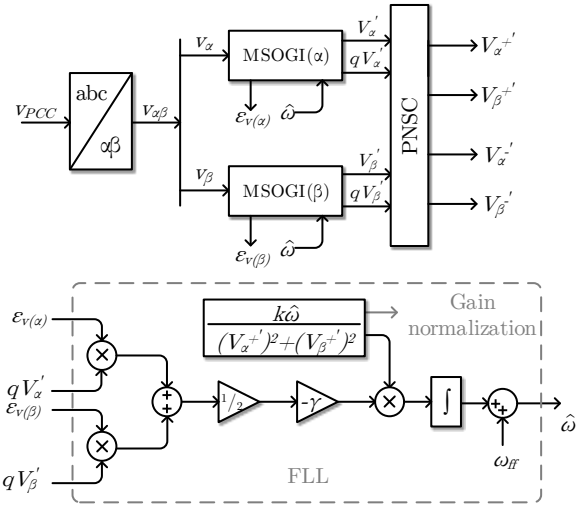


Fig. 6. Structure of the DMSOGI-FLL.

to obtain P_{cc}. The reference current in $\alpha\beta$ coordinates are obtained from the reactive power (Q^*) and modified active power ($P^* - P_{cc}$) using:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{(V_\alpha^{+\prime})^2 + (V_\beta^{+\prime})^2} \begin{bmatrix} V_\alpha^{+\prime} & -V_\beta^{+\prime} \\ V_\beta^{+\prime} & V_\alpha^{+\prime} \end{bmatrix} \begin{bmatrix} P^* - P_{cc} \\ Q^* \end{bmatrix} \quad (13)$$

where,

$$i_\alpha^* = \frac{V_\alpha^{+\prime}(P^* - P_{cc}) - V_\beta^{+\prime} Q^*}{(V_\alpha^{+\prime})^2 + (V_\beta^{+\prime})^2} \quad (14)$$

$$i_\beta^* = \frac{V_\beta^{+\prime}(P^* - P_{cc}) + V_\alpha^{+\prime} Q^*}{(V_\alpha^{+\prime})^2 + (V_\beta^{+\prime})^2}. \quad (15)$$

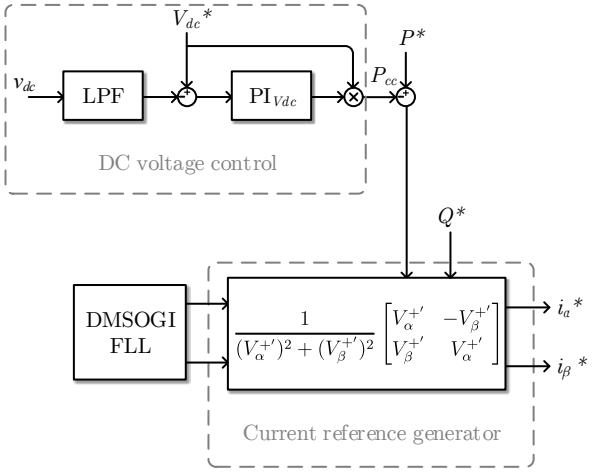


Fig. 7. PQ open-loop voltage control based on the stationary $\alpha\beta$ frame.

C. Current control

Stationary frame PI has been widely used for current control in three-phase systems. However, the PI controller fails in eliminate steady-state errors for ac quantities. In order to regulate the current in stationary reference, the Proportional Resonant controller (PR) is implemented in the system. The PR controller has been widely used for current regulation of grid-tied systems [16–19] due to the ability to eliminate de steady-state error between the controlled signal and its sinusoidal reference [19].

Additionally, the PR approach can be used to compensate the harmonics components cascading resonant blocks tuned to the desired harmonic order. The PR + HC (Proportional Resonant + Harmonic Compensator) block is presented in Fig. 8, where $G_{P+RES}(s)$ and $G_{hi}(s)$ are described:

$$G_{P+RES}(s) = K_p + \frac{2K_i s}{s^2 + \omega^2} \quad (16)$$

$$G_{hi}(s) = \sum_{h=3,5,7...} = \frac{2K_{hi} s}{s^2 + (h\omega)^2} \quad (17)$$

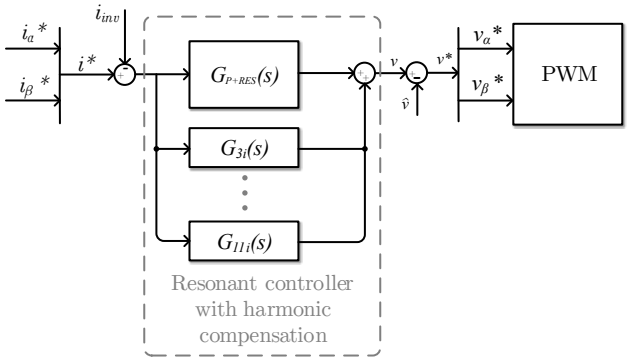


Fig. 8. Proportional Resonant (PR) control with harmonic compensation (HC).

The frequency response of PR+HC is shown in Fig. 9.

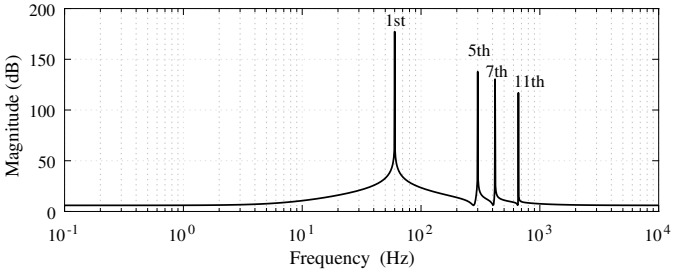


Fig. 9. Frequency response of PR controller with compensation in 5th, 7th and 11th harmonics.

D. Active Damping

The active damping is a technique that reduces the gain at resonant frequency in the LCL filter that increases the instability of the system in some cases [3]. In this way it increases the stability of system [20], [21]. When compared to passive damping its advantage is clear since it does not introduces losses in the power system, because it does not need a physical resistor in the filter circuit. The active damping could be implemented by two ways: by measure the capacitor current of LCL filter; or, by estimating it [7], [22], [23]. In this paper an estimation method is used based on [3].

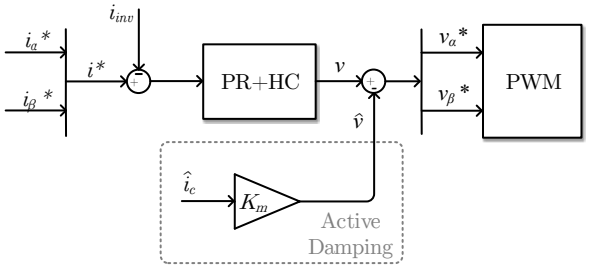
The diagram with active damping and the equivalent electrical circuit for obtaining the estimator for capacitor current are shown in Fig. 10 (a) and (b), respectively.

$$G_{PRAM_o}(s) = \frac{i_{inv}(s)}{i^* - i_{inv}} = \frac{a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5}{b_1 s^7 + b_2 s^6 + b_3 s^5 + b_4' s^4 + b_5' s^3 + b_6' s^2 + b_7' s} \tag{18}$$

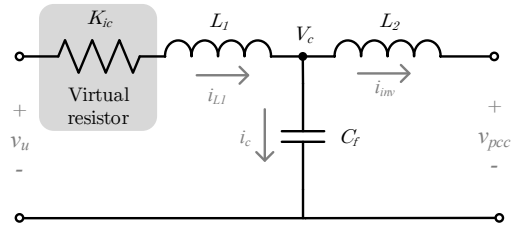
$$G_{PRAM_c}(s) = \frac{i_{inv}(s)}{i^*} = \frac{a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5}{b_1 s^7 + b_2 s^6 + b_3 s^5 + b_4 s^4 + b_5 s^3 + b_6 s^2 + b_7 s + b_8} \tag{19}$$

$$a_1 = K_p \quad a_2 = 2(Ki + K_{ih}) \quad a_3 = K_p\omega^2(1+h^2) \quad a_4 = 2\omega^2(K_i h^2 + K_{ih}) \quad a_5 = K_p\omega^4 h^2 \tag{20}$$

$$\begin{aligned}
b_1 &= CL_1L_{2r} & b_2 &= CK_mL_{2r} \\
b_3 &= CL_1L_{2r}(1+h^2)\omega^2 + L_1 + L_{2r} & b_4 &= K_p + CK_mL_{2r}(1+h^2)\omega^2 \\
b_5 &= 2(K_i + K_{ih}) + (L_1 + L_{2r})(1+h^2)\omega^2 + \omega^4 Ch^2 L_1 L_{2r} & b_6 &= K_p(1+h^2)\omega^2 + CK_mL_{2r}h^2\omega^4 \\
b_7 &= 2(K_i + K_{ih})\omega^2 + (K_p + L_1 + L_{2r})h^2\omega^4 & b_8 &= K_p h^2 \omega^4 \\
b_4' &= CK_mL_{2r}(1+h^2)\omega^2 & b_5' &= (L_1 + L_{2r})(1+h^2)\omega^2 + \omega^4 Ch^2 L_1 L_{2r} \\
b_6' &= \omega^2 + CK_mL_{2r}h^2\omega^4 & b_7' &= \omega^2 + (K_p + L_1 + L_{2r})h^2\omega^4
\end{aligned} \tag{21}$$



(a)



(b)

Fig. 10. Active damping: (a) block diagram and (b) equivalent electrical circuit for the LCL capacitor current estimation [3].

The estimation of capacitor current $\hat{i_c}$ is carried out adding a virtual resistor K_{ic} in series with the L_1 inductor of LCL filter. This resistor introduces a damping factor in the model such the estimation technique can be used with high resonance frequencies as in strong grids [3]. The estimation current is given by

$$\hat{i_c}(s) = \frac{v_u(s)Cs - i_{inv}(s)CL_1s^2 - i_{inv}(s)CK_{ic}s}{CL_1s^2 + CK_{ic}s + 1}, \tag{22}$$

where v_u can be approximated by voltage reference v^*. The design of parameters follows the approach taken by [3].

This paper introduces the three-phase case for the design of controller gains, that follows the approach presented in [3] for the single-phase case. Higher values for the gain (K_p) of proportional controller leads the closed loop system to present faster dynamic responses, while at the same time they can make the system unstable. Hence, the introduction of active damping and the proper adjust of its gain (K_m) allows flexibility in K_p gain variation. The combined design results in a better system performance for variations in grid parameters.

The model of the system without local load is presented in Fig. 11. L_{2r} represents the grid side inductor of LCL filter L_2 combined with the grid inductance L_{grid}. The open-loop ($G_{PRAM_O}(s)$) and closed-loop ($G_{PRAM_C}(s)$) transfer functions are obtained from this diagram. In this way it is possible to analyze the control approach in a wide range of grid parameters. Also, in order to implement the control

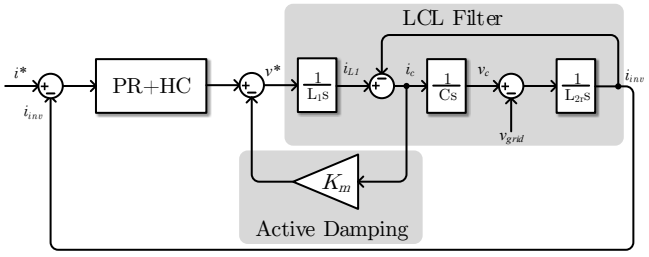


Fig. 11. System model for gains design.

First, it is important to analyze the impact of the variation of K_m, since its purpose is to increase the system stability and to reduce the gain of the LCL filter at resonance frequency. Fig. 12 shows the frequency response of (18) and Fig. 13 presents the root-locus of (19) in discrete-time for K_m variations. In this scenario, the proportional (K_p) and resonant gains (K_i, K_{ih}) of PR+HC are set 1 and 0, respectively, in order to analyze only the effect of active damping. Also, L_{2r} is considered to be equal to L_2 resulting in the most critical case of filter resonance. The active damping decrease the reference voltage v^* generated in current controller by $K_m\hat{i_c}$. Therefore, the $K_m\hat{i_c}$ is limited to 10% of the nominal voltage [24], resulting in a maximum $K_m = 10.4$. The increase of K_m leads the poles towards inside the unit circle, and provides damping attenuation in filter resonance as can been see in the Fig. 12 and 13, respectively. Hence, choosing $K_m = 2$ the active damping provides good attenuation and stability to the system, providing flexibility for further choice of K_p.

Fig. 14 and Fig. 15 show the impact of variation of K_p with

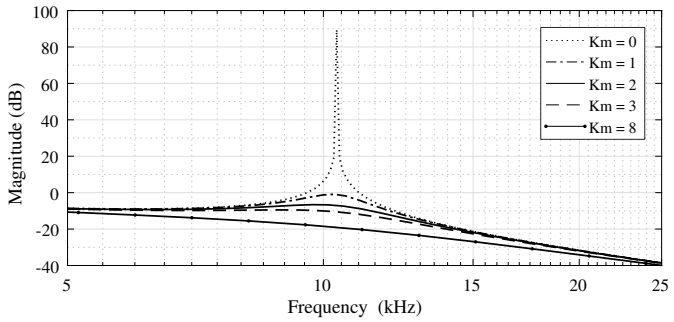


Fig. 12. Frequency response of $G_{PRAM_o}(s)$ for K_m variations.

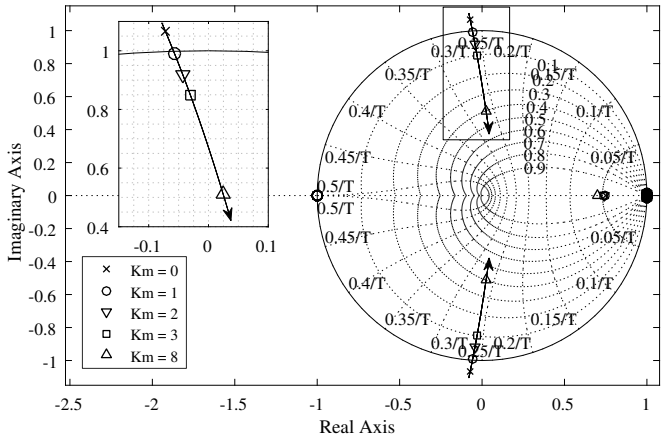


Fig. 13. Root locus of $G_{PRAM_c}(z)$ for K_m variations.

$K_m = 2$. The increase of K_p moves the poles toward outside the unit circle as it can be seen in Fig. 15. This increase causes the system to become unstable. Thus, the proportional gain of PR controller is set to $K_p = 2$. The integral gains of PR+HC are defined following the analysis carried out in [3]. The gains are chosen in order to reduce the steady state error and provide selectivity in the frequency. From this procedure, the integral resonant gain is set to $K_i = 3000$ and the harmonic resonant gains are set to $K_{ih} = 300$.

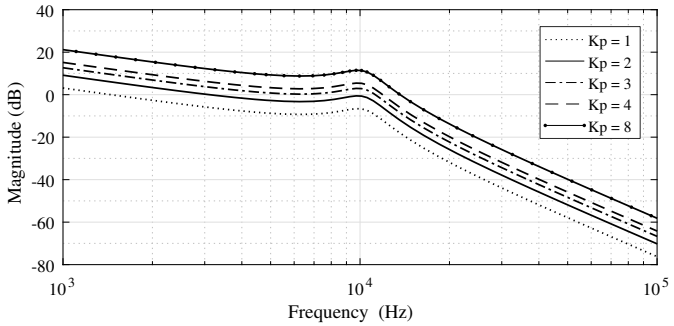


Fig. 14. Frequency response of $G_{PRAM_o}(s)$ for K_p variation.

IV. Applied Control Structure Analysis

The three-phase grid tied inverter of Fig. 1 is built under PSIM® environment in order to analyze the dynamic response of the control strategy (Fig. 2) designed in previous sections.

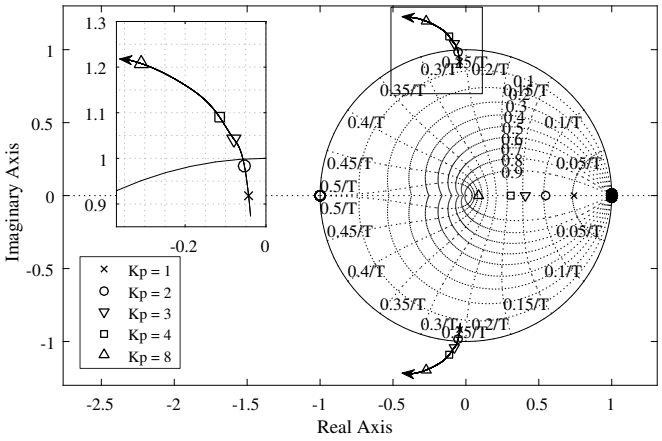


Fig. 15. Root locus of $G_{PRAM_c}(z)$ for K_p variation.

First, the PLL is tested under frequency, phase and voltage variation. Fig. 16 shows the response of DMSOGI-FLL when the PCC voltage is disturbed by both a phase-angle jump ($+20^o$) and a frequency variation (from 60 Hz to 61 Hz) at 150 ms and 200 ms respectively.

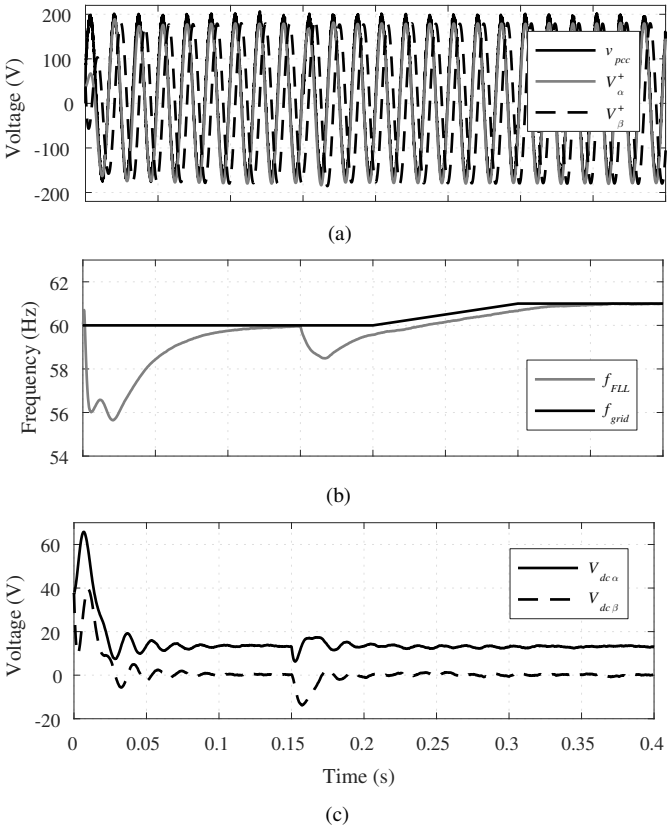


Fig. 16. DMSOGI-FLL under frequency and phase variation: (a) PCC phase voltage a, (b) Frequency estimation and (c) DC estimation.

In Fig. 16 (b), the frequency estimated (f_{FLL}) converges to the grid frequency (f_{grid}) in 150 ms after the variation at 200 ms. The convergence time is equal to the designed one in section III-A ($t_{s_{FLL}} = 150$ ms) and it is in accordance to the IEEE 1547 recommendations to detect abnormal frequencies. Moreover, in this evaluation scenario, an offset is included in

the sensor of phase a. The applied DMSOGI technique detects the 20 V offset, as shown in Fig. 16 (c).

Fig. 17 shows the response of DMSOGI under voltage variation. At 200 ms, the grid voltage is changed from 127 V (1 p.u.) to 0.8 p.u.. Both results (Fig. 16 (a) and Fig. 17 (a)) show the convergence of V_α^+ and V_β^+ under 24.4 ms as designed. The frequency estimation and DC rejection exhibits only a small variation at voltage jump as shown in Fig. 17 (b) and Fig. 17 (c).

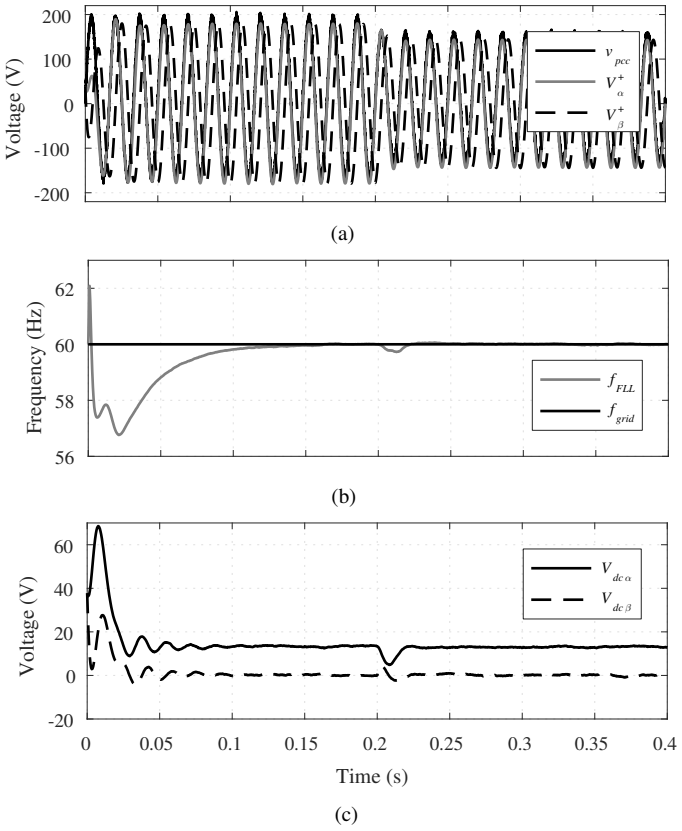


Fig. 17. DMSOGI-FLL under voltage variation. (a) PCC phase voltage a. (b) Frequency estimation. (c) DC estimation.

The current reference generator is also evaluated under power variation as shown in Fig. 18. Initially, active power (P^*) is gradually increased up to the maximum power of inverter (P_{inv} = 15 kW). After the instant 250 ms, the active and reactive power (Q^*) are step changed and the inverter current follows the required power.

Additionally, the effect of active damping is analyzed. Fig. 19 (a) and (b) present the effect of virtual resistor variation under strong (smaller inductance) and weak grid (large inductance), respectively. In both cases, after 100 ms the virtual resistor K_{ic} is changed from 4 to 0 which causes an error in current estimation. Consequently, the current and voltage at PCC exhibits a high frequency components due to resonance of the system.

Furthermore, Fig. 20 shows the comparison of inverter current total harmonic distortion (THD) for different approaches of active damping: by measure, by estimation and without active damping, for several grid inductances. In strong grids

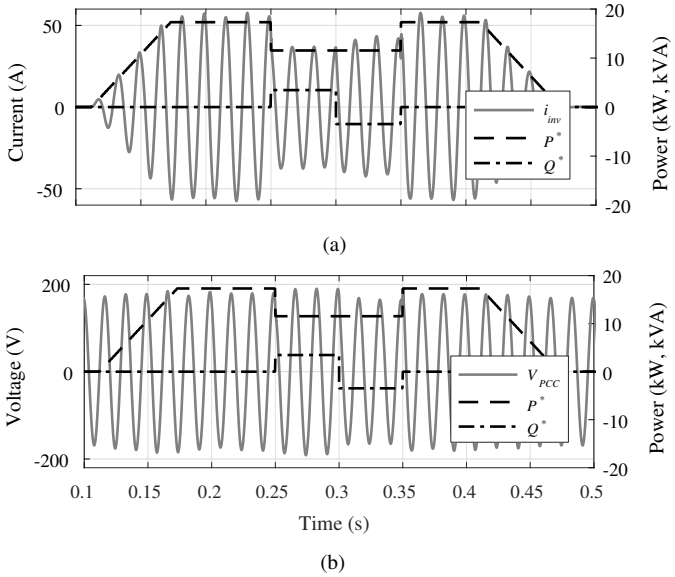


Fig. 18. Control of active and reactive power: (a) Inverter current at phase a and (b) PCC voltage at phase a.

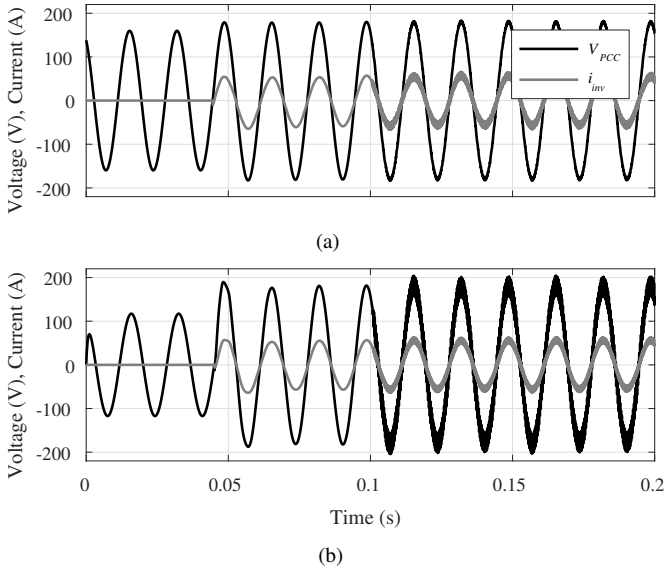


Fig. 19. Changes in virtual resistor (K_{ic}) for capacitor current estimation: (a) strong grid $L_g = 1\mu H$ and (b) weak grid $L_g = 3mH$.

(small inductance), which is the most critical case of filter resonance, the estimation technique presents a better performance than measure technique. And in weak grids the results are very similar. However, the current estimation has lower THD. In all cases the THD is lower than the 5% limit suggested by IEEE 1547.2-2018.

V. Conclusion

This paper proposed a general control structure for three-phase grid-tied inverters based on stationary frame. The control structure was designed to provide good performance under a wide range of the grid parameters. The DMSOGI-FLL technique allows the synchronization of inverter with the grid and eliminates the DC level that can arise in measurements.

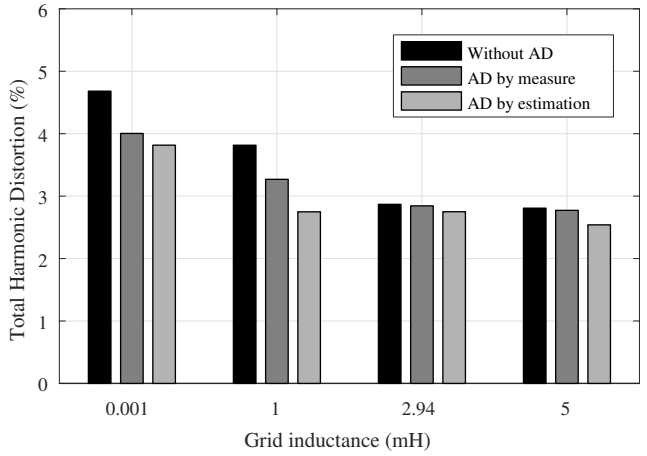


Fig. 20. Total harmonic distortion for grid inductance variation.

Active damping implementation allows higher gains in the current controller. Moreover, it reduces the current THD and increases the stability of the system for strong and weak grids.

The analysis demonstrates the robustness of the inverter under several scenarios and presented results within the limits suggested by IEEE 1547-2008 [5].

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