Space Vector Modulation for Packed-U-Cell Converters (PUC)

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***Abstract*—Generally, space vector modulation strategies employ the Three Nearest Vectors (NTV) to the reference voltage vector in order to achieve low distortion on the output voltages. When it comes to multilevel converters, the modulation technique must deal with a large number of redundancies and sometimes it must also perform the balance of the capacitor voltages, depending on the converter topology. This paper proposes a space vector modulation strategy applied to Packed-U-Cell Converters (PUC). It is proposed a cost function to be minimized comprising two objectives: (i) adjacent switching vectors distance minimization (ii) desired currents in order to keep the capacitors charged. The proposed cost function minimization results in a optimized switching sequence and balanced capacitor voltages. Simulation results demonstrate the good performance of the proposed modulation strategy.**

***Keywords* – Space Vector Modulation Pulse-Width Modulation (SV-PWM), Multilevel Inverter, Packed-U-Cell Converters (PUC).**

I. Introduction

Multilevel converters have experienced a widespread employment due to its advantageous features [1]–[3]. Among these advantages are the reduced voltage over the devices and better spectra of the output voltages. Currently, the main multilevel topologies are: Neutral Point Clamped (NPC) [4], [5], Flying Capacitor Converter (FLC) [6], [7], Cascaded H-bridge (CHB) [8] and Modular Multilevel Converter (MMC) [9]. Furthermore, academy and industry have adopted multilevel converters for several applications such as: motor drives, renewable energy and active filter [10].

Recently the Packed U-cell (PUC) was proposed as a multilevel topology option [11]. When compared to classic multilevel converters, this topology presents less switches for the same number of voltage levels. As a disadvantage, it presents asymmetric reverse block voltages across the semiconductors. Similar structures with generalization for converters with high number of levels have been presented by [12], [13].

In [14] a control and modulation strategy was proposed in order to dismiss voltage sensors for the PUC. In [15] a Model Predictive Controller (MPC) is proposed, applied to a PUC. The strategy results in seven output voltage levels, however the MPC does not restrict the use of the nearest voltage vectors, which penalize the spectra of the output voltages.

Space Vector Pulse-Width Modulation (SVPWM) approaches provide a degree of freedom to select switching vectors, making it possible to obtain output voltages with reduced THD and low switching losses [16]. Furthermore, by a proper design, it is possible to regulate the capacitor voltages in multilevel converters [17], [18]. On the other hand, multilevel converters can present challenges to handle a great number of redundancies.

This paper proposes a space vector modulation strategy applied to Packed-U-Cell Converters (PUC) (Figure 1). From the nearest three vectors algorithm, a set of redundant vectors is defined. Therefore, it is proposed a method to select a feasible switching sequence in order to reduce the switching losses and to balance the capacitor voltages. These aims are achieved by means a cost function minimization comprising both vector distance and capacitor current criteria. Finally, simulation results are obtained to demonstrate the good performance of the proposed modulation strategy.

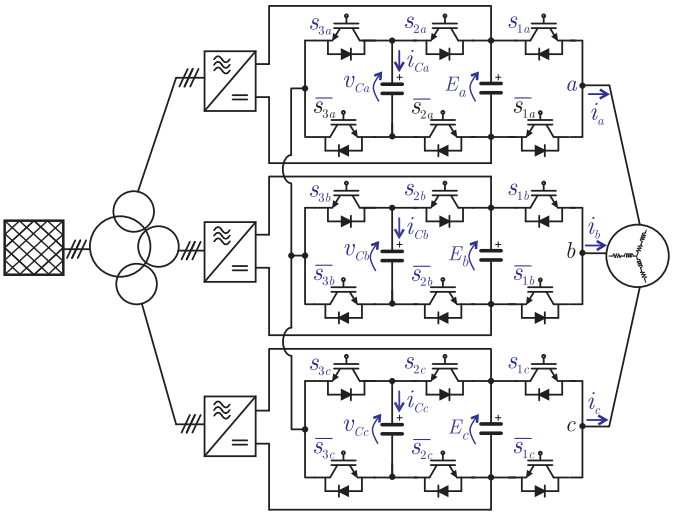

Fig. 1. Three-Phase Five Level Packed-U-Cell Converter-PUC5.

II. Description of the Proposed Modulation Strategy

Generally, modulation strategies applied to multilevel converters comprehend some objectives as:

(i) Minimize the switching losses of the power semiconductor devices;

(ii) Improve the THD and WTHD indexes by eliminating or minimizing harmonic components associated with the output variables such as voltages and currents;
(iii) Promote the equilibrium of the voltages of floating capacitors, depending on the converter topology.

The PUC5 [19] has five output voltage levels per phase according to Table I, where x represent the output phase $x = \{a, b, c\}$. It can be seen that there are some redundant voltage vectors. This means that different switching states synthesize the same output voltage, but they result in opposite current flowing through the phase capacitor.

TABLE I
PHASE SWITCHING STATES OF PUC5.

State	S_{1x}	S_{2x}	S_{3x}	i_{Cx}	v_x/E_x	v_x
1	0	1	1	0	$-E_x$	-1
2	0	1	0	$-i_x$	$v_{Cx} - E_x$	-1/2
3	0	0	1	i_x	$-v_{Cx}$	
4	0	0	0	0	0	0
5	1	1	1			
6	1	0	1	i_x	$E_x - v_{Cx}$	1/2
7	1	1	0	$-i_x$	v_{Cx}	
8	1	0	0	0	E_x	1

The three-phase PUC5 of Figure 1 has 2^9 possible switching vectors. These switching vectors are denoted by $\mathbf{v}_s^k$, as:

$$\mathbf{v}_s^k = \begin{bmatrix} S_{1a} & S_{2a} & S_{3a} & S_{1b} & S_{2b} & S_{3b} & S_{1c} & S_{2c} & S_{3c} \end{bmatrix}^T \tag{1}$$

where k=1,2,3...2^9, and $S_{1a}...S_{3c}$ are the state of the switches which can assume 0 for OFF-state or 1 for ON-state. The set of all vectors $\mathbf{v}_s$ is called U_s. On the other hand, here are defined the vectors $\mathbf{v}_f$ belonging to the set U_f and the vectors $\mathbf{v}_l$ belonging to the set U_l. The vectors $\mathbf{v}_f$ represent the phase converter voltages while $\mathbf{v}_l$ represent the phase-to-phase converter voltages. The vectors $\mathbf{v}_s^k$ which belongs to the set U_s can be mapped into the sets U_f and U_l by means of the linear operators F_f and F_l:

$$F_f = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{2}$$

$$F_l = \begin{bmatrix} 2 & -1 & -1 & -1 & \frac{1}{2} & \frac{1}{2} & -1 & \frac{1}{2} & \frac{1}{2} \\ -1 & \frac{1}{2} & \frac{1}{2} & 2 & -1 & -1 & -1 & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3}$$

Therefore, $\mathbf{v}_f^k$ and $\mathbf{v}_l^k$ can be written as function of $\mathbf{v}_s^k$ as:

$$\begin{aligned} \mathbf{v}_f^k &= \frac{N}{E} F_f \mathbf{v}_s^k + N[\mathbf{1}]_{3\times 1} \\ \mathbf{v}_l^k &= \frac{N}{E} F_l \mathbf{v}_s^k + N[\mathbf{1}]_{2\times 1}, \end{aligned} \tag{4}$$

with N=0.5$(M-1)$, where M is the number of levels of the converter (in this case $M = 5$) and $[\mathbf{1}]_{n\times 1}$ is the unity vector. Furthermore, (4) can be related with the phase and phase-to-phase output converter voltages as (5) and (6) respectively:

$$\mathbf{v}_f^k = \frac{N}{E} \begin{bmatrix} v_a^k & v_b^k & v_c^k \end{bmatrix}^T + N[\mathbf{1}]_{3\times 1}, \tag{5}$$

$$\mathbf{v}_l^k = \frac{N}{E} \begin{bmatrix} v_{ab}^k & v_{bc}^k \end{bmatrix}^T + N[\mathbf{1}]_{2\times 1}, \tag{6}$$

By means of this mapping, all voltage vector belonging to the sets U_f and U_l can be determined.

A. Nearest Three Vectors Identification (NTV)

When it comes to three-phase three-wire systems, the sum of all output voltages is equal to zero, therefore, without any loss of generality, a two-dimensional coordinate system can be used to represent them. Usually, SV modulation strategies use the three nearest vectors in order to synthesize output voltages with low harmonic content. The identification of the nearest vectors can be performed similarly to [20]. The nearest four vectors in the phase-to-phase coordinate system [21] are selected by the following rounding functions

$$\begin{aligned} \mathbf{v}_{ul} &= \begin{bmatrix} \text{ceil}(v_{ab}^*) & \text{floor}(v_{bc}^*) \end{bmatrix}^T \\ \mathbf{v}_{lu} &= \begin{bmatrix} \text{floor}(v_{ab}^*) & \text{ceil}(v_{bc}^*) \end{bmatrix}^T \\ \mathbf{v}_{ll} &= \begin{bmatrix} \text{floor}(v_{ab}^*) & \text{floor}(v_{bc}^*) \end{bmatrix}^T \\ \mathbf{v}_{uu} &= \begin{bmatrix} \text{ceil}(v_{ab}^*) & \text{ceil}(v_{bc}^*) \end{bmatrix}^T. \end{aligned} \tag{7}$$

Figure 2 shows the voltage reference and the nearest vectors derived from (7) while Figure 3 shows a normalized two-dimensional SV diagram, with the voltage vectors (black dots) and a sinusoidal reference voltage vector $\mathbf{v}^*$ (red dots).

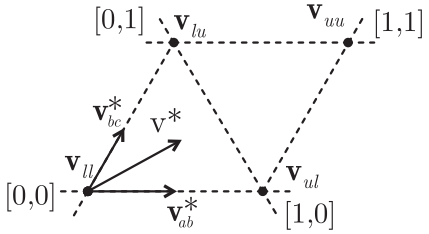

Fig. 2. Nearest Three Vectors Identification (NTV).

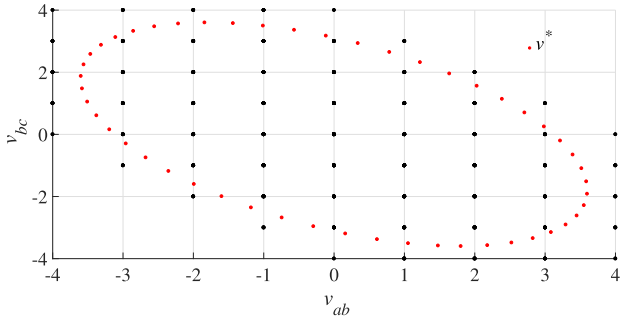

Fig. 3. Normalized two-dimensional SV diagram.

Here, the vectors $\mathbf{v}_1$ and $\mathbf{v}_2$ represent two of the three nearest vectors to the reference. The third vector $\mathbf{v}_3$ is defined by analyzing the signal of $\mathbf{v}_{ab}^* + \mathbf{v}_{bc}^* - (\mathbf{v}_{ul_{ab}} + \mathbf{v}_{ul_{bc}})$. If

positive, the three nearest vectors and its duty cycles are, respectively:

$$\begin{aligned} \mathbf{v}_1 &= \mathbf{v}_{ul}, \quad d_1 = -(\mathbf{v}^*_{bc} - \mathbf{v}_{uu_{bc}}) \\ \mathbf{v}_2 &= \mathbf{v}_{lu}, \quad d_2 = -(\mathbf{v}^*_{ab} - \mathbf{v}_{uu_{ab}}) \\ \mathbf{v}_3 &= \mathbf{v}_{uu}, \quad d_3 = 1 - d_1 - d_2. \end{aligned} \tag{8}$$

Otherwise, the three nearest vectors and its duty cycles are, respectively:

$$\begin{aligned} \mathbf{v}_1 &= \mathbf{v}_{ul}, \quad d_1 = -(\mathbf{v}^*_{ab} - \mathbf{v}_{ll_{ab}}) \\ \mathbf{v}_2 &= \mathbf{v}_{lu}, \quad d_2 = -(\mathbf{v}^*_{bc} - \mathbf{v}_{ll_{bc}}) \\ \mathbf{v}_3 &= \mathbf{v}_{ll}, \quad d_3 = 1 - d_1 - d_2. \end{aligned} \tag{9}$$

Note that $\mathbf{v}_1$, $\mathbf{v}_2$, $\mathbf{v}_3$ are voltage vectors in phase-to-phase coordinates, i.e $\mathbf{v} = [v_{ab} \; v_{bc}]^T$, and the next step of the algorithm is to define all redundant switching vectors. One way to find these states is evaluating (10) as:

$$\begin{aligned} \mathbf{v}^k_{1f} &= \begin{bmatrix} k & k - v_{1ab} & 1 - v_{1ab} - v_{1bc} \end{bmatrix}^T \\ \mathbf{v}^k_{2f} &= \begin{bmatrix} k & k - v_{2ab} & 1 - v_{2ab} - v_{2bc} \end{bmatrix}^T \\ \mathbf{v}^k_{3f} &= \begin{bmatrix} k & k - v_{3ab} & 1 - v_{3ab} - v_{3bc} k \end{bmatrix}^T, \end{aligned} \tag{10}$$

where $k, k - v_{ab}, 1 - v_{ab} - v_{bc} \in [0, N-1]$. Thus, by means of (10) a set of all redundant vectors in phase coordinates is found.

B. Definition of the switching sequences

Generally, the switching sequences must result in reduced switching losses and low output distortion [16]. Therefore, the use of two redundant vectors in adjacent positions in a switching sequence is avoided. Commonly, a switching sequence presents four vectors, where the first and the last are redundant. In order to result in lower switching losses (reduced number of switch transitions), two adjacent switching vectors must have the minimal euclidean distance between them [21]. The euclidean distance $D \in \mathbb{R}^9$ between two generic switching vectors $\mathbf{v}^k_s$ and $\mathbf{v}^{(k+1)}_s$ is given by

$$D = \sqrt{\left(\mathbf{v}^k_s - \mathbf{v}^{(k+1)}_s\right)^T \cdot \left(\mathbf{v}^k_s - \mathbf{v}^{(k+1)}_s\right)}. \tag{11}$$

Therefore, the first step is to define the first vector of the sequence. Let us suppose that there are no previous sequence, then a vector with one redundancy at least must be selected. Once the first vector of this sequence, $\mathbf{v}_{s1}$, is defined, the second vector $\mathbf{v}_{s2}$ with the lower distance to the first is selected as

$$D_j = \sqrt{\left(\mathbf{v}_{s1} - \mathbf{v}^j_{s2}\right)^T \cdot \left(\mathbf{v}_{s1} - \mathbf{v}^j_{s2}\right)}. \tag{12}$$

Once selected the second vector for minimal D_j, the next step is to seek $\mathbf{v}_{s3}$ as

$$D_j = \sqrt{\left(\mathbf{v}_{s2} - \mathbf{v}^j_{s3}\right)^T \cdot \left(\mathbf{v}_{s2} - \mathbf{v}^j_{s3}\right)}. \tag{13}$$

In a similar way the next step consists in selecting the vector $\mathbf{v}_{s4}$ as

$$D_j = \sqrt{\left(\mathbf{v}_{s3} - \mathbf{v}^j_{s4}\right)^T \cdot \left(\mathbf{v}_{s3} - \mathbf{v}^j_{s4}\right)}. \tag{14}$$

It can be pointed out that the first and the fourth vector are redundant, hence they implement the same output phase-to-phase voltage. Moreover, the last vector of a sequence and the first vector of the next sequence must have the minimal D. This procedure results in reduced number of commutations, however it does not ensure the balance of the capacitor voltages.

C. Control of the capacitor voltages and description of the cost function

In order to control the capacitor voltages v_{Ca}, v_{Cb} and v_{Cc}, a proportional-integrator PI is used. The output of the PI is the desired reference current to ensure the voltage according to the reference $v_{Cx} = E_x/2$ (see Figure 4). To reduce the switching losses while controlling the capacitor voltages, a generalized cost function is presented here, composed by the distance criteria previously defined and a second parcel responsible for the voltage capacitor control, i.e.

$$J_j = \lambda_d \sqrt{\mathbf{d}^T_j \mathbf{d}_j} + \lambda_c \sum_{p=1}^{3} \sum_{l=1}^{L} \left(\left| i^*_{Cplj} - i_{Cplj} \right| \right), \tag{15}$$

where p is phase number and l is the number of capacitor per phase of the converter and

$$\mathbf{d} = \mathbf{v}^k_s - \mathbf{v}^{(k+1)}_s. \tag{16}$$

For a three-phase converter with one capacitor per phase, (15) can be simplified as

$$\begin{aligned} J_j = \lambda_d D_j + \lambda_c (& \left| i^*_{Caj} - i_{Caj} \right| + \left| i^*_{Cbj} - i_{Cbj} \right| \cdots \\ & \cdots + \left| i^*_{Ccj} - i_{Ccj} \right|). \end{aligned} \tag{17}$$

In (17), the constants λ_d and λ_c are the weights for each parcel in the cost function. Therefore, the vectors $\mathbf{v}_y$ for $y = \{1, 2, 3, 4\}$ of the switching sequence is defined by the minimization of the cost function (17) as:

$$\mathbf{v}_y = \min \{J_j\} \tag{18}$$

Figure 4 shows the block diagram of the proposed SV strategy.

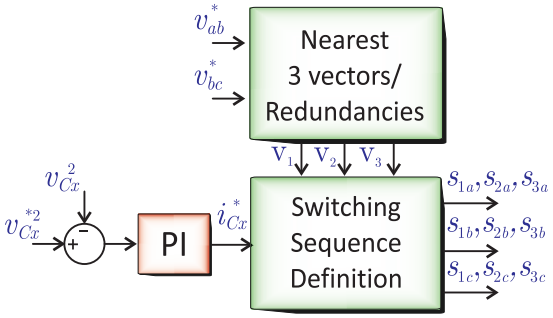

Fig. 4. Block diagram of the proposed modulation strategy.

III. Simulation Results

In order to demonstrate the performance of the proposed space vector strategy, simulation results from a 25 kW from a three-phase PUC5 feeding an RL load are presented. The main parameters are: phase capacitors C_x=0.5 mF, dc-link voltages E_x=600 V, fundamental frequency f_1=60 Hz, switching frequency f_s=3 kHz.

Figures 5 and 6 show the output PWM voltages and output currents for a modulation index m_a=0.9. The three nearest space vector naturally results in phase-to-phase output voltages with nearest step voltage levels.

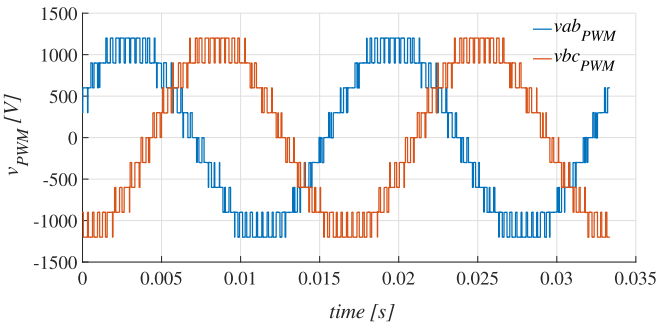

Fig. 5. Phase-to-phase output voltages in steady state.

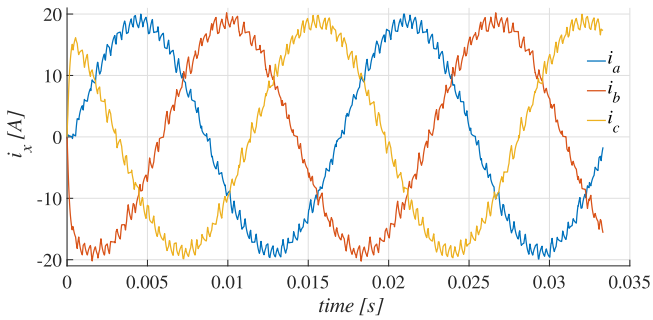

Fig. 6. Output currents in steady state.

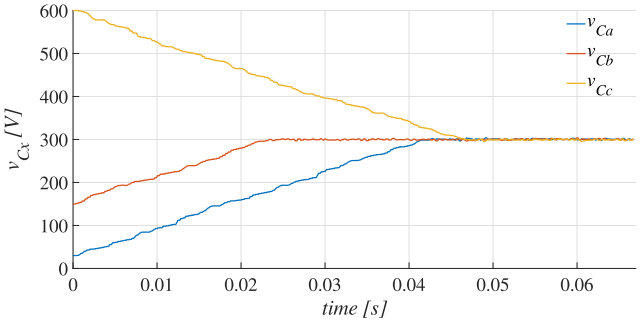

Fig. 7. Convergence of the capacitor voltages starting from unbalanced values.

Figure 7 shows the capacitor voltage convergence starting from unbalanced values. The capacitor voltages become equal to $E_x/2$ at a reduced time interval demonstrating the good performance in terms of capacitor voltages control.

In order to evaluate the behavior of the converter under the variation of input voltage, it was applied a step in the dc bus voltage from 600V to 800V. The phase-to-phase output voltages, the output currents and the capacitor voltages are shown in Figures 8, 9, 10, respectively. Once the reference of the capacitor voltages are one half of the dc input, they reach 400V in a short period after the step change.

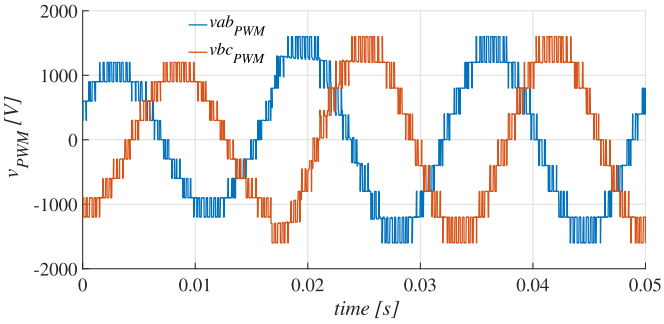

Fig. 8. Phase-to-phase output voltages during a step in the input dc bus.

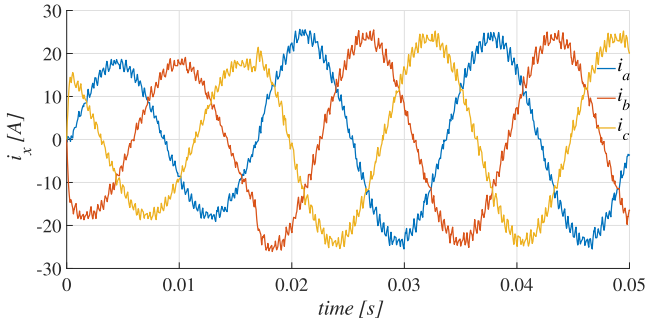

Fig. 9. Output currents during a step in the input dc bus.

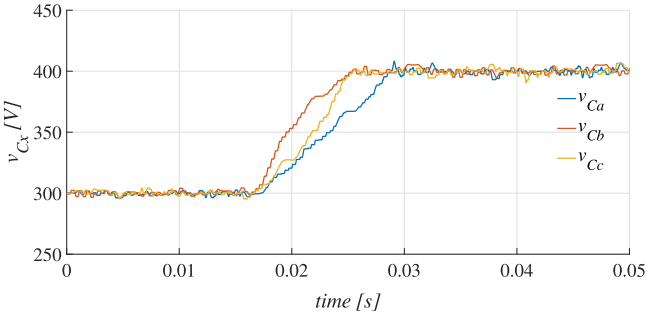

Fig. 10. Capacitor voltages during a step in the input dc bus.

In order to demonstrate the impact of weights λ_d and λ_c on the switching signals, two scenarios were evaluated where the total number of transitions of the switches was accounted by the index nc (number of commutations). For this analysis, a time window of three sample periods ($3/f_s$) and the

modulation index $m_a = 0.7$ were adopted. Figure 11 shows the switching signals for $\lambda_d = 1$ and $\lambda_c = 100$ while Figure 12 shows the switching signals for $\lambda_d = 100$ and $\lambda_c = 1$. It can be seen that a large λ_d (Figure 12) result in $nc = 31$ while a small λ_c results in $nc = 42$ (Figure 11). Furthermore, with lower λ_d more than one switch commutates simultaneously.

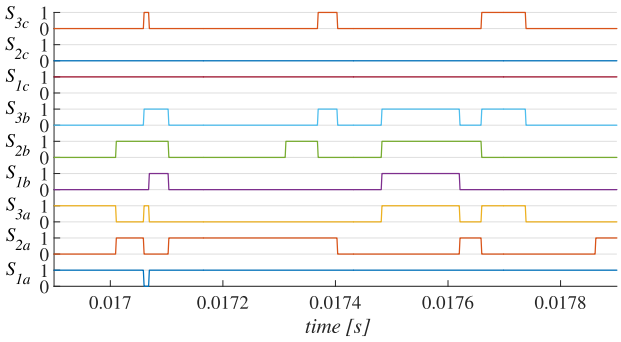

Fig. 11. Switching signals for $\lambda_d = 1$ and $\lambda_c = 100$, ($nc = 42$).

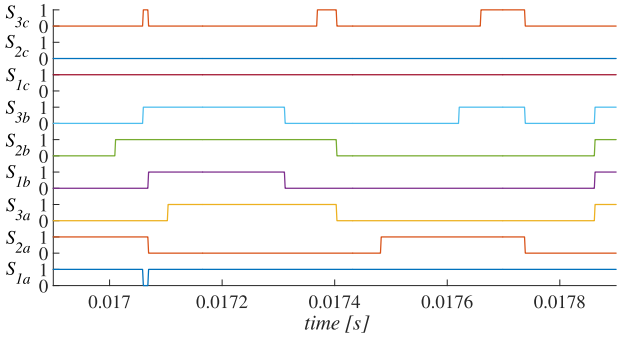

Fig. 12. Switching signals for $\lambda_d = 100$ and $\lambda_c = 1$, ($nc = 31$).

The weighting factor design depends on the analysis of performance indexes. Here, the indexes are nc (number of switch commutations) and vcf (capacitor voltage fluctuation) are used to define λ_d and λ_c. The index vcf is defined as

$$vcf = 100 \cdot \frac{|E_x/2 - v_{Cx}|}{E_x/2}. \tag{19}$$

where v_{Cx} is the voltage capacitor of the phase x. This index gives the capacitor voltage deviation from its nominal value. A feasible way to define the weights can be derived from curves which relates λ_d and λ_c with nc and vcf. Figure 13 shows the index vcf (mean value over a fundamental period) for different λ_d and λ_c as function of the modulation index. There are five combinations of λ_d and λ_c expressed by five curves. Although the five curves are very close to each other, it is possible to note that $\lambda_c > \lambda_d$ leads to a small vcf. Figure 14 shows nc for different λ_d and λ_c as function of the modulation index m_a in a fundamental period. Note that for $\lambda_d > \lambda_c$ results in lower nc. From the Figures 13 and 14, it is possible infer that $\lambda_d = 100$ and $\lambda_c = 1$ leads to good results in terms of nc without compromising the performance of vcf.

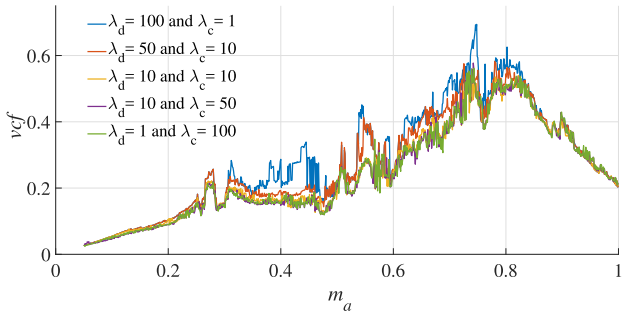

Fig. 13. Voltage capacitor fluctuation for a fundamental period.

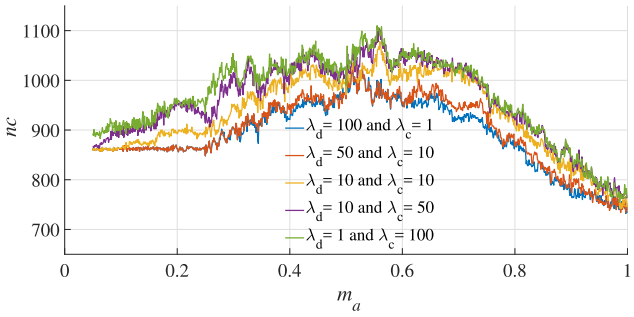

Fig. 14. Number of commutations nc for different λ_d and λ_c in a fundamental period.

Fig. 15 shows the Total Harmonic Distortion (THD) of the phase-to-phase output voltage for different λ_d and λ_c. Note that all curves are overlapped, evidencing the non dependence of λ_d and λ_c over the THD. Once the space vector strategy is based on three nearest vectors, the THD is unchanged by the use of different redundant vectors.

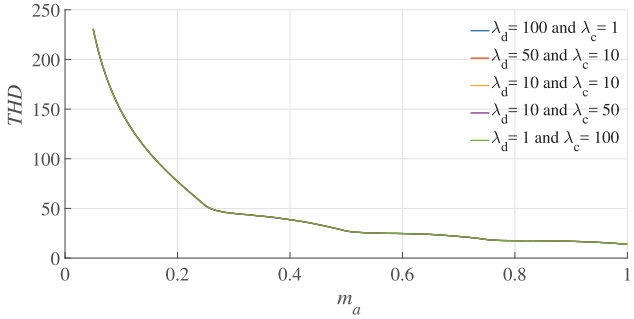

Fig. 15. Total Harmonic Distortion of v_{ab}.

IV. Conclusion

This paper has presented a space vector modulation strategy for three-phase five level Packed-U-Cell converters. The proposed modulation strategy provides the reduction switching transitions by using the adjacent vectors distance criteria while keeping balanced the capacitors voltage. By minimizing a defined cost function both indexes related to switching losses

and capacitor voltage fluctuation can be reduced. Moreover, this strategy can easily expanded to further multilevel converter which employs floating capacitors. Simulation results was presented to demonstrate the good performance of the proposed technique.

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